

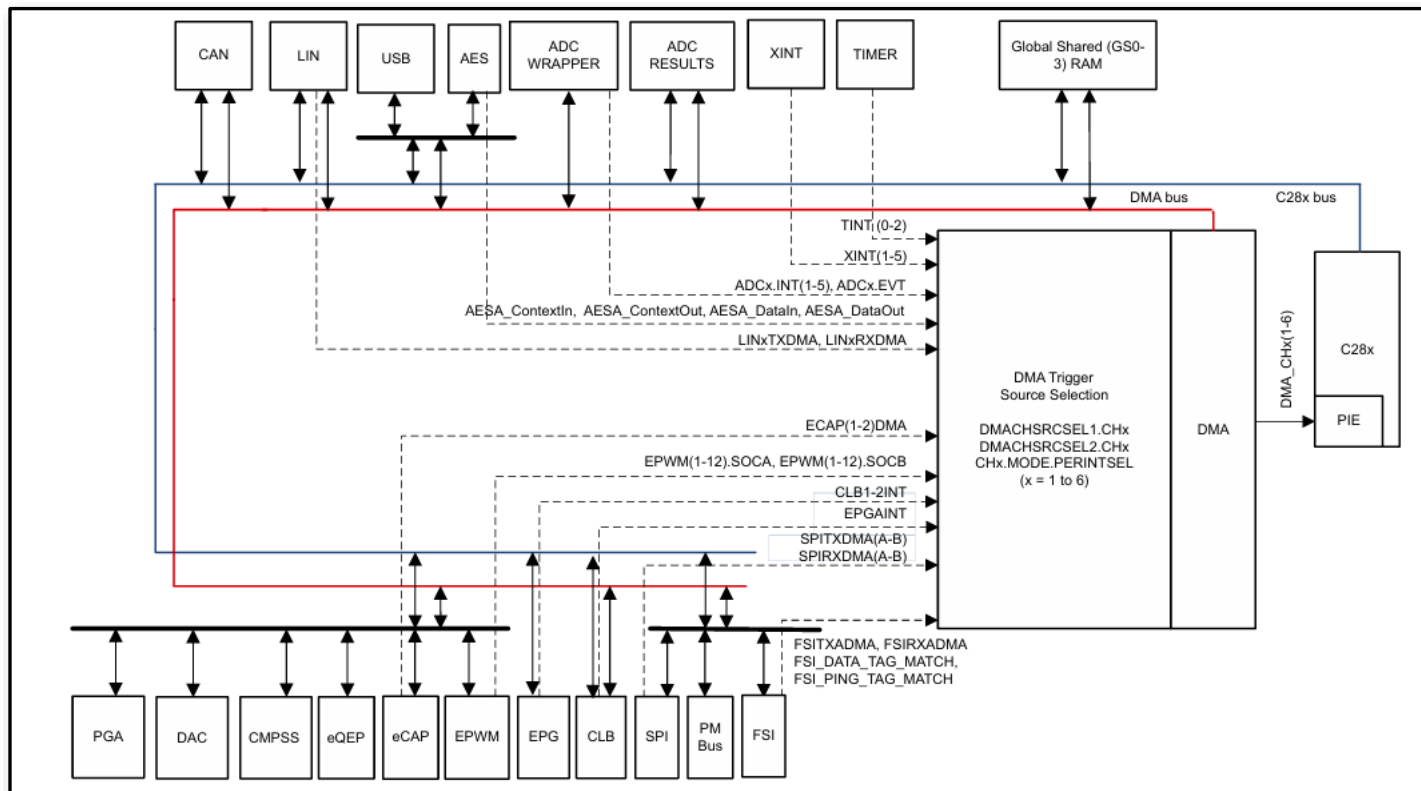
F28P55x编程实例Labs_DMA

- Code Composer Studio
- C2000Ware
- LaunchXL-F28P55x

DMA

Direct Memory Access, 直接存储器访问

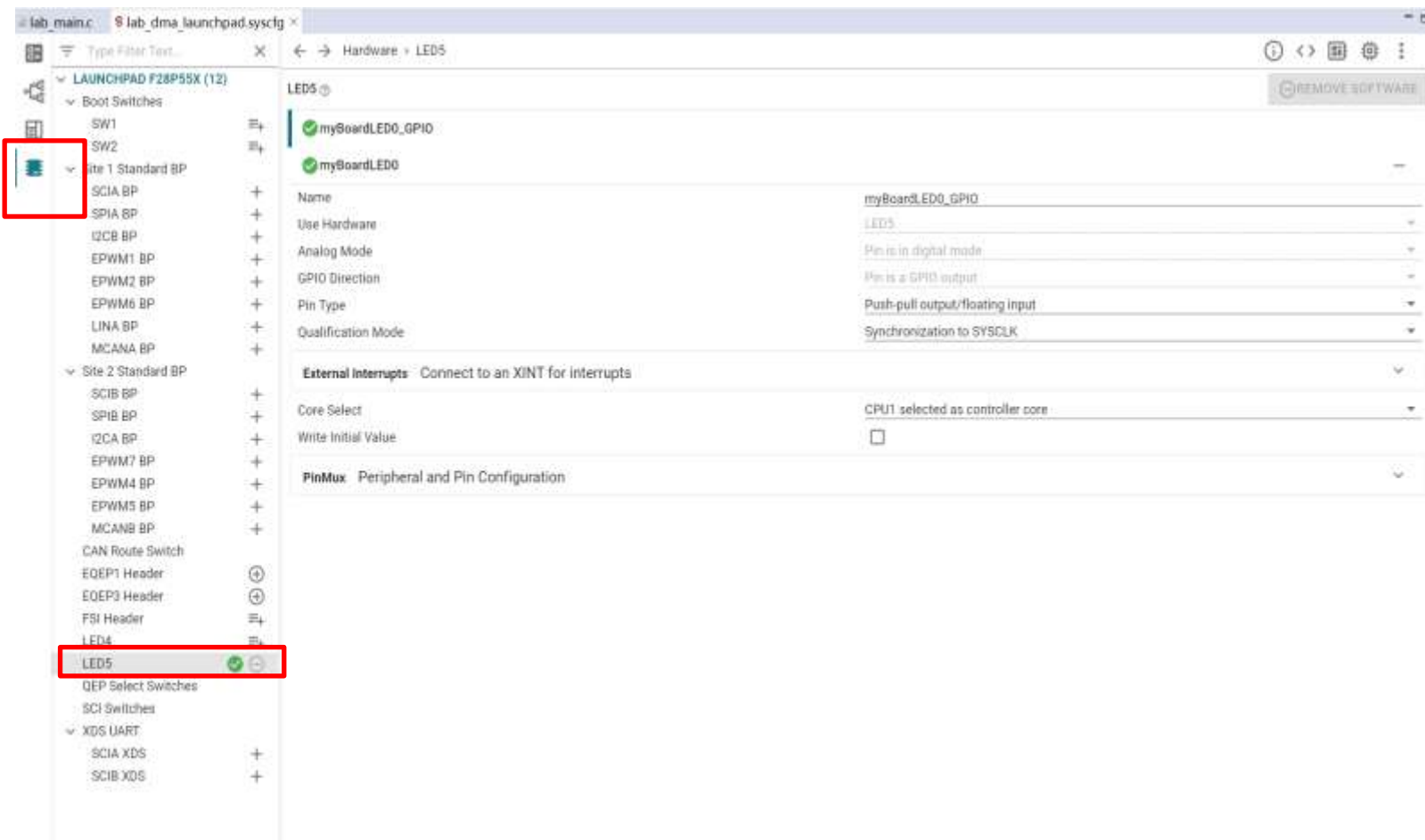
- 外设和存储器之间，无需CPU干预
- 有六个独立的PIE中断
- 外设中断触发源丰富
 - ① ADC中断和EVT信号
 - ② 外部中断
 - ③ EPWM SOC信号
 - ④ CPU计时器
 - ⑤ ECAP
 - ⑥ SPI发送/接收
 - ⑦ LIN发送/接收
- 数据源和目标
 - ① ADC结果寄存器
 - ② 控制外设：EPWM、EQEP、ECAP
 - ③ 通讯外设：SPI、LIN、CAN、PMBus、USB
 - ④ PAG控制寄存器
- 字大小：16/32，每个字4个周期，无需仲裁



DMA

配置LED

GPIO	用途
LED5	运行状态指示



DMA

配置EPWM1

The screenshot shows the TI Configurator interface for configuring EPWM1. The left sidebar displays a system tree with various components. The 'EPWM' component is highlighted with a red box. The main window shows the configuration for 'EPWM (2 of 12 Added)', including 'myEPWM0' and 'myEPWM1'. The 'EPWM Time Base' section is expanded, showing various settings such as Emulation Mode, Time Base Clock Divider, High Speed Clock Divider, Time Base Period Load Mode, Time Base Period Load Event, Time Base Period, Time Base Period Link, Enable Time Base Period Global Load, and Initial Counter Value. The 'Initial Counter Value' is set to 0. The 'EPWM Global Load' section is also visible, showing 'Load EPWM Settings From Device Memory Export' and 'Copy Settings' options.

lab_dma_launchpad.syscfg

Software > EPWM

SYSTEM (18)

- AID
- CLA
- CLB INPUTXBAR INPUT
- CLB OUTPUTXBAR
- CLBXBAR
- CPUTIMER 1/3
- DCC
- EPWMXBAR
- ERAD
- FLASH
- GPIO 1/66
- INPUTXBAR INPUT
- INTERRUPT 1
- MEMCFG
- OTHER
- OUTPUTXBAR
- SYSCTL
- WATCHDOG

ANALOG (6)

- ADC 1/5
- ANALOG PinMux 1/1
- ASYSCTL 1/1
- CMPSS
- DAC
- PGA

CONTROL (5)

- CLB
- EPAP
- EPWM 3/12**
- EQEP
- SYNC 1/1

COMMUNICATION (10)

- DMA 1/6
- FSIRX

Global Parameters Settings that affect all instances

EPWM (2 of 12 Added)

- myEPWM0
- myEPWM1

Name myEPWM0

Use Hardware None

Load EPWM Settings From Device Memory Export

Copy Settings

Template Code Generation

EPWM Global Load

EPWM Time Base

Emulation Mode Stop after next Time Base counter increment or decrement

Time Base Clock Divider Divide clock by 1

High Speed Clock Divider Divide clock by 1

Time Base Period Load Mode For perfectly synchronized TBCLKs across multiple EPWM modules, the prescaler bits in the TBCTL register of each EPWM module must be set identically

Time Base Period Load Event Divide clock by 1

Time Base Period PWM Period register access is through shadow register

Time Base Period Link Shadow to active load occurs when time base counter reaches 0

Enable Time Base Period Global Load 25000

Initial Counter Value Disable Linking

0

DMA

配置EPWM1

$$\text{Time Base Period} = \frac{f_{clk}}{2f_{pwm}} = \frac{100 \times 10^6}{2 \times 2000} = 25000.$$

$$\text{Counter Compare Value} = \left(1 - \frac{duty}{100}\right) * tbprd = \left(1 - \frac{25}{100}\right) * 25000 = 18750.$$

EPWM Time Base

Emulation Mode

Time Base Clock Divider

High Speed Clock Divider

Time Base Period Load Mode

Time Base Period Load Event

Time Base Period

Time Base Period Link

Enable Time Base Period Global Load

Initial Counter Value

Counter Mode

Counter Mode After Sync

Enable Phase Shift Load

Force a Sync Pulse

Sync In Pulse Source

Sync Out Pulse

One-Shot Sync Out Trigger

EPWMxSYNCPER Source Select

Stop after next Time Base counter increment or decrement

Divide clock by 1

1 For perfectly synchronized TBCLKs across multiple EPWM modules, the prescaler bits in the TBCTL register of each EPWM module must be set identically.

Divide clock by 1

PWM Period register access is through shadow register

Shadow to active load occurs when time base counter reaches 0

25000

Disable Linking

0

Up - down - count mode

Count down after sync event

Sync-in source is EPWM1 sync-out signal

None

Trigger is OSHT sync.

Counter equals Period

EPWM Counter Compare

CMPA

Counter Compare A (CMPA)

Enable Counter Compare A (CMPA) Global Load

Enable Shadow Counter Compare A (CMPA)

Counter Compare A Shadow Load Event

18750

! It is recommended to use a non-zero counter compare value when using shadow to active load of action qualifier A/B control register on TBCTR=0 boundary(Un-suppress)

Load when counter equals zero

配置EPWM1

EPWM Counter Compare	
EPWM Action Qualifier	
Enable Continuous SW Force Global Load	<input type="checkbox"/>
Continuous SW Force Shadow Mode	Shadow mode load when counter equals zero
T1 Trigger Source	Digital compare event A 1 <i>T1/T2 selection and configuration of a trip/digital-compare event is independent of the configuration of that event in the Trip-Zone submodule</i>
T2 Trigger Source	Digital compare event A 1 <i>T1/T2 selection and configuration of a trip/digital-compare event is independent of the configuration of that event in the Trip-Zone submodule</i>
ePWMxA Output Configuration	
ePWMxA Global Load Enable	<input type="checkbox"/>
ePWMxA Shadow Mode Enable	<input checked="" type="checkbox"/>
ePWMxA Shadow Load Event	Load when counter equals zero
ePWMxA One-Time SW Force Action	No change in the output pins
ePWMxA Continuous SW Force Action	Software forcing disabled
ePWMxA Event Output Configuration	
ePWMxA Time base counter equals zero	No change in the output pins
ePWMxA Time base counter equals period	No change in the output pins
ePWMxA Time base counter up equals COMPA	Set output pins to High
ePWMxA Time base counter down equals COMPA	Set output pins to low
ePWMxA Time base counter up equals COMPB	No change in the output pins
ePWMxA Time base counter down equals COMPB	No change in the output pins
ePWMxA T1 event on count up	No change in the output pins
ePWMxA T1 event on count down	No change in the output pins
ePWMxA T2 event on count up	No change in the output pins
ePWMxA T2 event on count down	No change in the output pins

PinMux Qualification ▾

PinMux Peripheral and Pin Configuration ^

EPWM Peripheral	EPWM1	▾ 🔒
EPWM_A	GPIO0/79 (EPWM1 BP)	▾ 🔒
	⚠ Connected to hardware(Un-suppress).	
EPWM_B	GPIO1/78 (EPWM1 BP)	▾ 🔒
	⚠ Connected to hardware(Un-suppress).	

DMA

配置EPWM2

The screenshot shows the TI Configurator interface for configuring EPWM2. The left sidebar displays a tree view of system components, with 'EPWM' (2/12) highlighted under the 'CONTROL' category. The main panel shows the configuration for 'myEPWM1'. A red box highlights the 'ADD' button in the top right corner of the configuration area. The configuration parameters are as follows:

Parameter	Value
Name	myEPWM1
Use Hardware	None
Emulation Mode	Stop after next Time Base counter increment or decrement
Divide clock by	1
Time Base Clock Divider	1
High Speed Clock Divider	1
Time Base Period Load Mode	PWM Period register access is through shadow register
Time Base Period Load Event	Shadow to active load occurs when time base counter reaches 0
Time Base Period	1999
Time Base Period Link	Disable Linking
Enable Time Base Period Global Load	<input type="checkbox"/>
Initial Counter Value	0
Counter Mode	Up-count mode

EPWM Time Base	^
Emulation Mode	Stop after next Time Base counter increment or decrement
Time Base Clock Divider	Divide clock by 1 <i>i</i> For perfectly synchronized TBCLKs across multiple EPWM modules, the prescaler bits in the TBCTL register of each EPWM module must be set identically
High Speed Clock Divider	Divide clock by 1
Time Base Period Load Mode	PWM Period register access is through shadow register
Time Base Period Load Event	Shadow to active load occurs when time base counter reaches 0
Time Base Period	1999
Time Base Period Link	Disable Linking
Enable Time Base Period Global Load	<input type="checkbox"/>
Initial Counter Value	0
Counter Mode	Up - count mode
Enable Phase Shift Load	<input type="checkbox"/>
Force a Sync Pulse	<input type="checkbox"/>
Sync In Pulse Source	Sync-in source is EPWM1 sync-out signal
Sync Out Pulse	None
One-Shot Sync Out Trigger	Trigger is OSHT sync
EPWMxSYNCPER Source Select	Counter equals Period

$$\text{Time Base Period} = \frac{f_{tbclk}}{2f_{sym}} = \frac{100 \times 10^6}{2 \times 25300} = 2000.$$

DMA

配置EPWM2

EPWM Event-Trigger ⓘ	
Enable EPWM Interrupt	<input type="checkbox"/>
ADC SOC Trigger	
SOCA Trigger Enable	<input checked="" type="checkbox"/>
SOCA Trigger Source	Time-base counter equal to zero or period
SOCA Trigger Event Count	1 Event Generates Interrupt
SOCA Trigger Event Count Initial Value Load Enable	<input type="checkbox"/>
SOCB Trigger Enable	<input type="checkbox"/>
HRPWM	
PinMux Use Case	ALL
PinMux Qualification	
PinMux Peripheral and Pin Configuration	
EPWM Peripheral	EPWM2
EPWM_A	GPIO2/77 (EPWM2 BP) ⚠ Connected to hardware(Un-suppress)
EPWM_B	GPIO3/76 (EPWM2 BP) ⚠ Connected to hardware(Un-suppress)

DMA

配置ADC

lab_main.c lab_dma_launchpad.sysctf

Type Filter Text...

- SYSTEM (18)
 - AIO
 - CLA
 - CLB INPUTXBAR INPUT
 - CLB OUTPUTXBAR
 - CLBXBAR
 - CPUTIMER 1/3
 - DCC
 - EPWMXBAR
 - ERAD
 - FLASH
 - GPIO 1/66
 - INPUTXBAR INPUT
 - INTERRUPT 1
 - MEMCFG
 - OTHER
 - OUTPUTXBAR
 - SYSTL
 - WATCHDOG
- ANALOG (6)**
 - ADC 1/3**
 - ANALOG Pin Mux 1/1
 - ASYSCTL 1/1
 - CMPSS
 - DAC
 - PGA
- CONTROL (5)
 - CLB
 - ECAP
 - EPWM 2/12
 - EQEP
 - SYNC 1/1
- COMMUNICATION (10)
 - DMA 1/6
 - FSIRX
 - FSITX
 - I2C

ADC (1 of 5 Added)

+ ADD

= REMOVE ALL

myADC0

Name	myADC0
ADC Instance	ADCA
ADC Clock Prescaler	ADCCLK = (input clock) / 4.0
Enable alternate timings (tDMA)	<input checked="" type="checkbox"/>
Use External MUX	<input type="checkbox"/>
High Priority Mode SOCs	Round robin mode is used for all

SOC Configurations Start of Conversion Configurations

Enable SOCs	SOC/EOC number 0
-------------	------------------

SOC0 Start of Conversion 0

SOC0 Name	SOC0
SOC0 Independent Name Mode	<input type="checkbox"/>
SOC0 Channel	single-ended, ADCIN0
SOC0 Module Channel Name	A0
SOC0 Device Pin Name	23: A0/ B15/ C15/ DACA_OUT
SOC0 External Channel Selected via MUX	ADC_CH_ADCINX_0

SOC Triggers

Trigger Mode	Single Trigger
SOC0 Trigger	ePWM2, ADCSOCA
SOC0 Interrupt Trigger	No ADCINT will trigger the SOC

Sample Time Calculator

SOC0 Sample Window [SYSCLK counts]	8 ⚠ SOC0 sample window must be at least 10(Un-suppress)
SOC0 Sample Time [ns]	53.333333333333336

12

ADC INT Configurations Interrupt Configurations

ADC Interrupt Pulse Mode Occurs at the end of the conversion

Enable ADC Interrupts **ADCINT1 Interrupt**

INT1 ADC Interrupt 1

Enable ADC Interrupt 1

Interrupt 1 SOC Source SOC/EOC0

Continuous Interrupt Mode

PPB Configurations Post Processing Blocks Configurations

Burst Mode ADC Burst Mode

Register PIE Interrupt Handlers

Use Interrupt

Register Interrupts None

Analog PinMux myANALOGPinMux0

Name myANALOGPinMux0

Use Case CUSTOM

Pins Used **A0, B15, C15, DACA_OUT**

PinMux Peripheral and Pin Configuration

DMA

配置ADC

The screenshot shows the TI Configurator interface for configuring the ANALOG PinMux. The left sidebar lists various system components, with 'ANALOG PinMux' highlighted in a red box. The main panel displays the configuration for 'myANALOGPinMux0'. The 'Use Case' is set to 'CUSTOM', and the 'Pins Used' dropdown menu is highlighted in a red box, showing the selected pins: 'A0, B15, C15, DACA_OUT'.

The screenshot shows the TI Configurator interface for configuring the ASYSCTL. The left sidebar lists various system components, with 'ANALOG PinMux' and 'ASYSCTL' highlighted in a red box. The main panel displays the configuration for 'ASYSCTL'. The 'Analog Reference' section is expanded, and the 'Analog Reference Voltage' dropdown menu is highlighted in a red box, showing the selected voltage: '1.65V'.

DMA

配置DMA

The screenshot displays the TI Configurator interface for configuring a DMA channel. The left sidebar shows a tree view of components, with 'DMA' highlighted under 'COMMUNICATION (18)'. The main configuration area shows the following settings for 'myDMA0':

- Name: myDMA0
- DMA Channel: DMA CH1
- Enable Triggers:
- Trigger Source: TRIGGER ADCA1
- Use Interrupt:
- Register Interrupt Handler:
- Enable Interrupts:
- Enable Overrun Interrupt:
- Interrupt Mode: DMA interrupt is generated at the beginning of a transfer
- Emulation Mode: Continue DMA operation regardless of emulation suspend
- One-Shot Configuration: Only one burst transfer performed per trigger.
- Continuous Mode Configuration: DMA reinitializes when the transfer count is zero and waits for a trigger.
- Databus Width: DMA transfers 16 bits at a time.
- Burst Size: 1
- Transfer Size: 50
- Number of words to be transferred: 50
- Enable Channel 1 Priority:
- Start Channel:

Source Address Setup Source address setup options

- Source Address Input Type: Variable/Function Name
- Source Address Variable: AdcAddr
- Source Wrap Size: 50
- Source Address Wrap Step: 0

Destination Address Setup Destination address setup options

DMA Interrupt

- Name: myDMA0_INT
- Interrupt Name: INT_myDMA0
- Interrupt Handler: dma_Ch1ISR
- Enable interrupt in PIE:

DMA

配置Timer

The screenshot shows the TI Studio IDE interface with the following components:

- Top Tab Bar:** lab_main.c, lab_dma_launchpad.syscfg, device.c, sysctl.h
- Left Panel (Component Tree):** SYSTEM (18) expanded to show various components. The **CPUTIMER** component is highlighted with a red box, showing a count of 1/3 and a green checkmark.
- Right Panel (Configuration):** CPUTIMER (1 of 3 Added) configuration for **myCPUTIMER0**.
 - Name:** myCPUTIMER0
 - CPUTIMER Instance:** CPUTIMER0
 - Emulation Mode:** Denotes that the timer will stop after the next decrement
 - Timer Prescaler:** 0
 - Timer Period:** 4294967295
 - Enable Interrupt:**
 - Register Interrupt Handler:**
 - Start Timer:**

DMA

