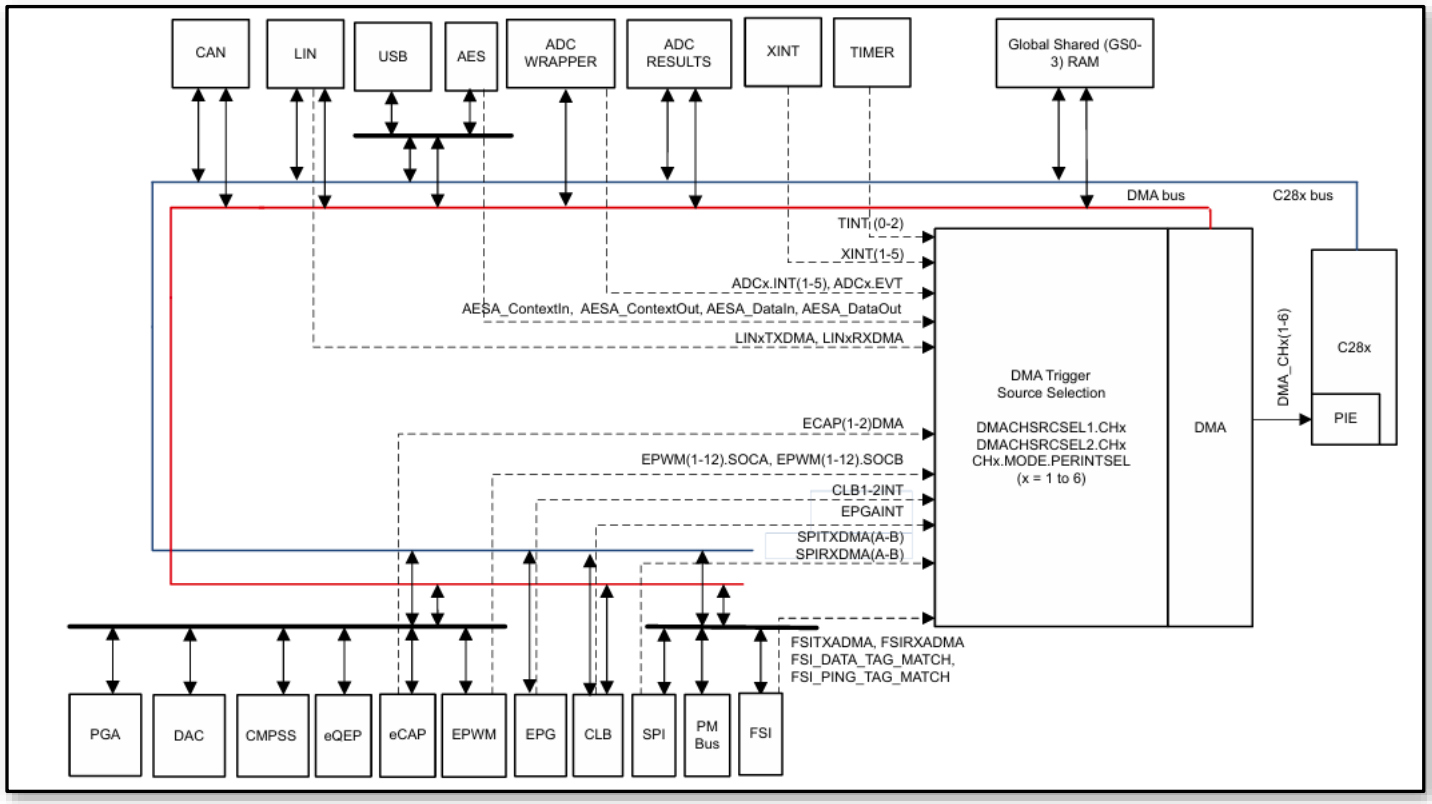
F28P55x编程实例Labs_DMA

- Code Composer Studio
- C2000Ware
- LaunchXL-F28P55x

DMA

Direct Memory Access，直接存储器访问

- 外设和存储器之间，无需CPU干预
- 有六个独立的PIE中断
- 外设中断触发源丰富
  ①ADC中断和EVT信号
  ②外部中断
  ③EPWM SOC信号
  ④CPU计时器
  ⑤ECAP
  ⑥SPI发送/接收
  ⑦LIN发送/接收
- 数据源和目标
  ① ADC结果寄存器
  ②控制外设：EPWM、EQEP、ECAP
  ③通讯外设：SPI、LIN、CAN、PMBus、USB
  ④PAG控制寄存器
- 字大小：16/32，每个字4个周期，无需仲裁



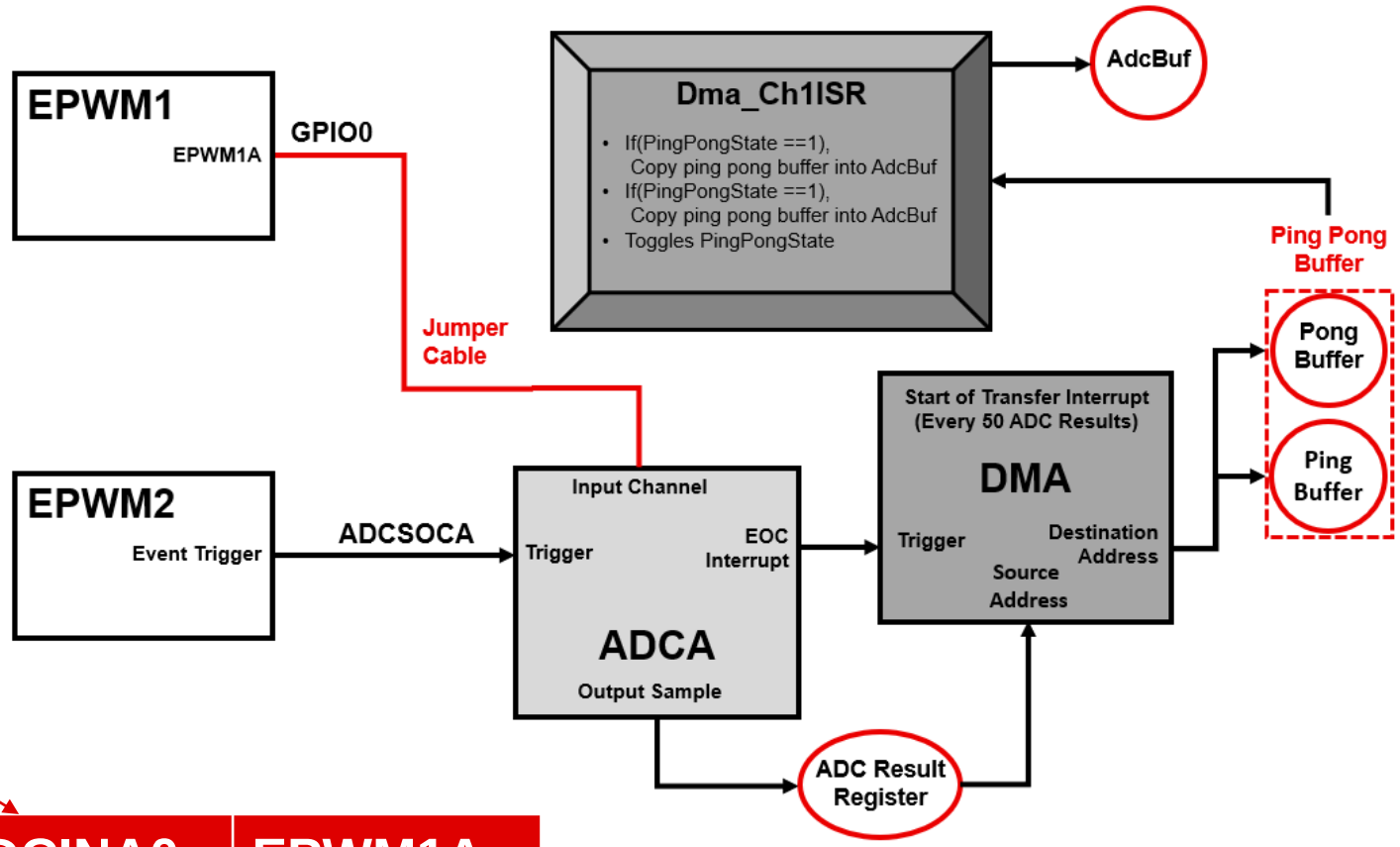
DMA

功能实现

EPWM1产生PWM波形，ADC采集PWM,
EPWM2用来触发ADC采样，
ADC采样中断触发DMA,
DMA把数据存入AdcBuf

实现步骤

- EPWM1--- GPIOA0
- 复制空白工程
- Sysconfig配置EPWM1
- Sysconfig配置EPWM2
- Sysconfig配置ADC
- Sysconfig配置DMA
- Sysconfig配置Timer
- 编写应用代码

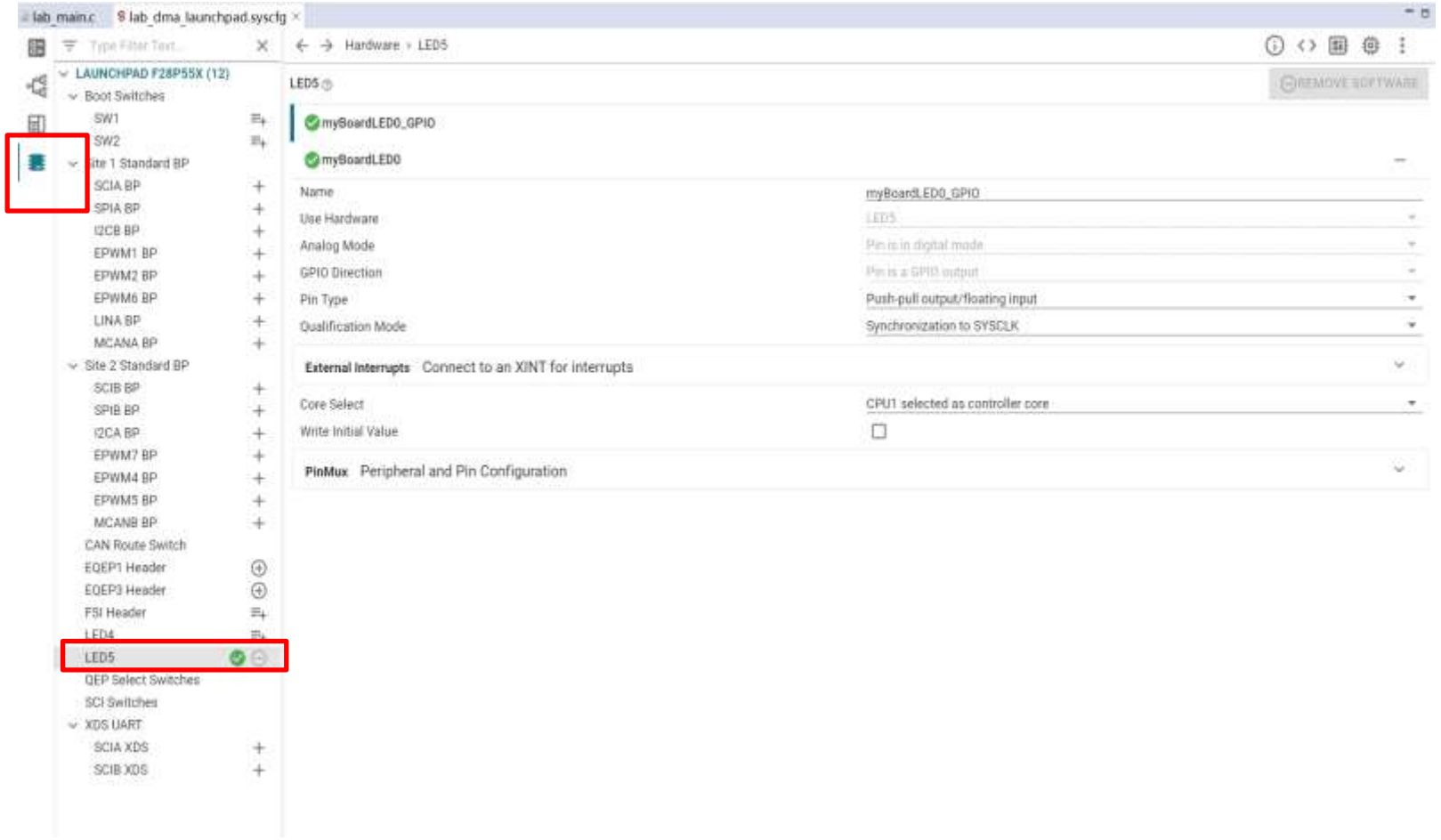


资源名称	ADCINA0	EPWM1A
PIN脚	70	40

DMA

GPIO	用途
LED5	运行状态指示

配置LED



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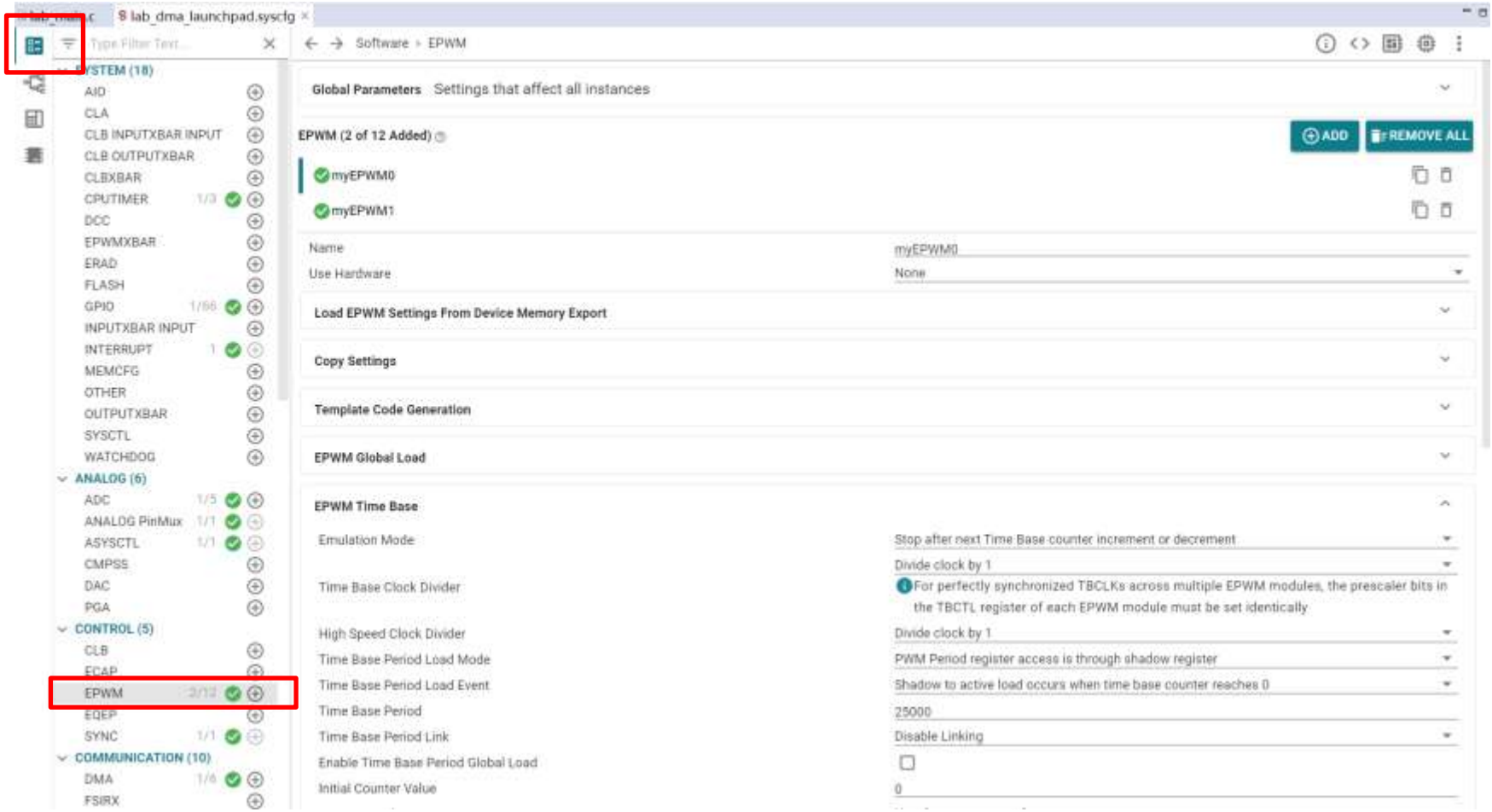
配置EPWM1



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配置EPWM1

$$\text{Time Base Period} = \frac{f_{tbclk}}{2f_{pwm}} = \frac{100*10^6}{2*2000} = 25000.$$

$$\text{Counter Compare Value} = (1 - \frac{duty}{100}) * tbprd = (1 - \frac{25}{100}) * 25000 = 18750.$$

EPWM Time Base

Emulation Mode	Stop after next Time Base counter increment or decrement
Time Base Clock Divider	Divide clock by 1
	For perfectly synchronized TBCLKs across multiple EPWM modules, the prescaler bits in the TBCTL register of each EPWM module must be set identically
High Speed Clock Divider	Divide clock by 1
Time Base Period Load Mode	PWM Period register access is through shadow register
Time Base Period Load Event	Shadow to active load occurs when time base counter reaches 0
Time Base Period	25000
Time Base Period Link	Disable Linking
Enable Time Base Period Global Load	☐
Initial Counter Value	0
Counter Mode	Up - down - count mode
Counter Mode After Sync	Count down after sync event
Enable Phase Shift Load	☐
Force a Sync Pulse	☐
Sync In Pulse Source	Sync-in source is EPWM1 sync-out signal
Sync Out Pulse	None
One-Shot Sync Out Trigger	Trigger is OSHT sync
EPWMxSYNCPER Source Select	Counter equals Period

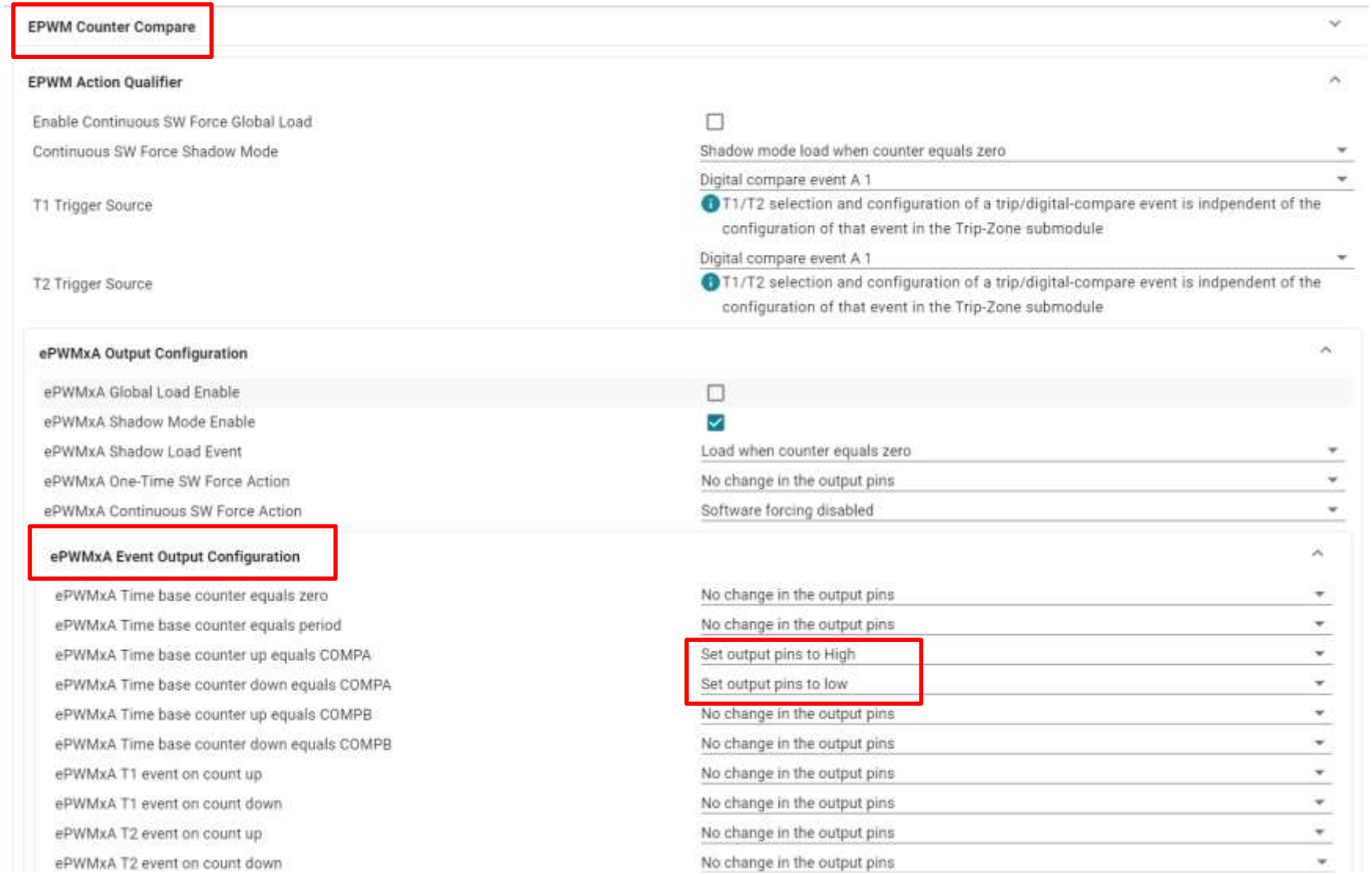
EPWM Counter Compare

CMPA

Counter Compare A (CMPA)	18750
	It is recommended to use a non-zero counter compare value when using shadow to active load of action qualifier A/B control register on TBCTR=0 boundary(Un-suppress)
Enable Counter Compare A (CMPA) Global Load	☐
Enable Shadow Counter Compare A (CMPA)	☑
Counter Compare A Shadow Load Event	Load when counter equals zero

DMA

配置EPWM1



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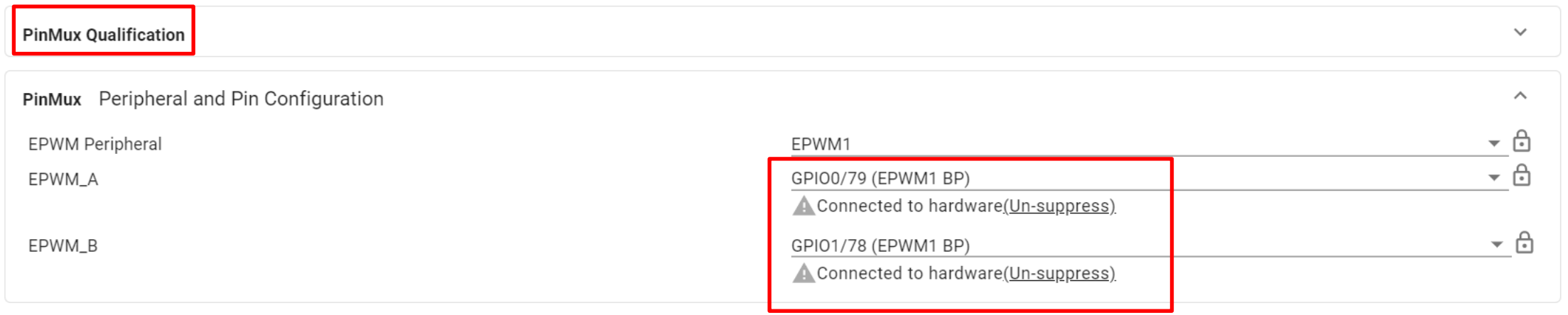
配置EPWM1



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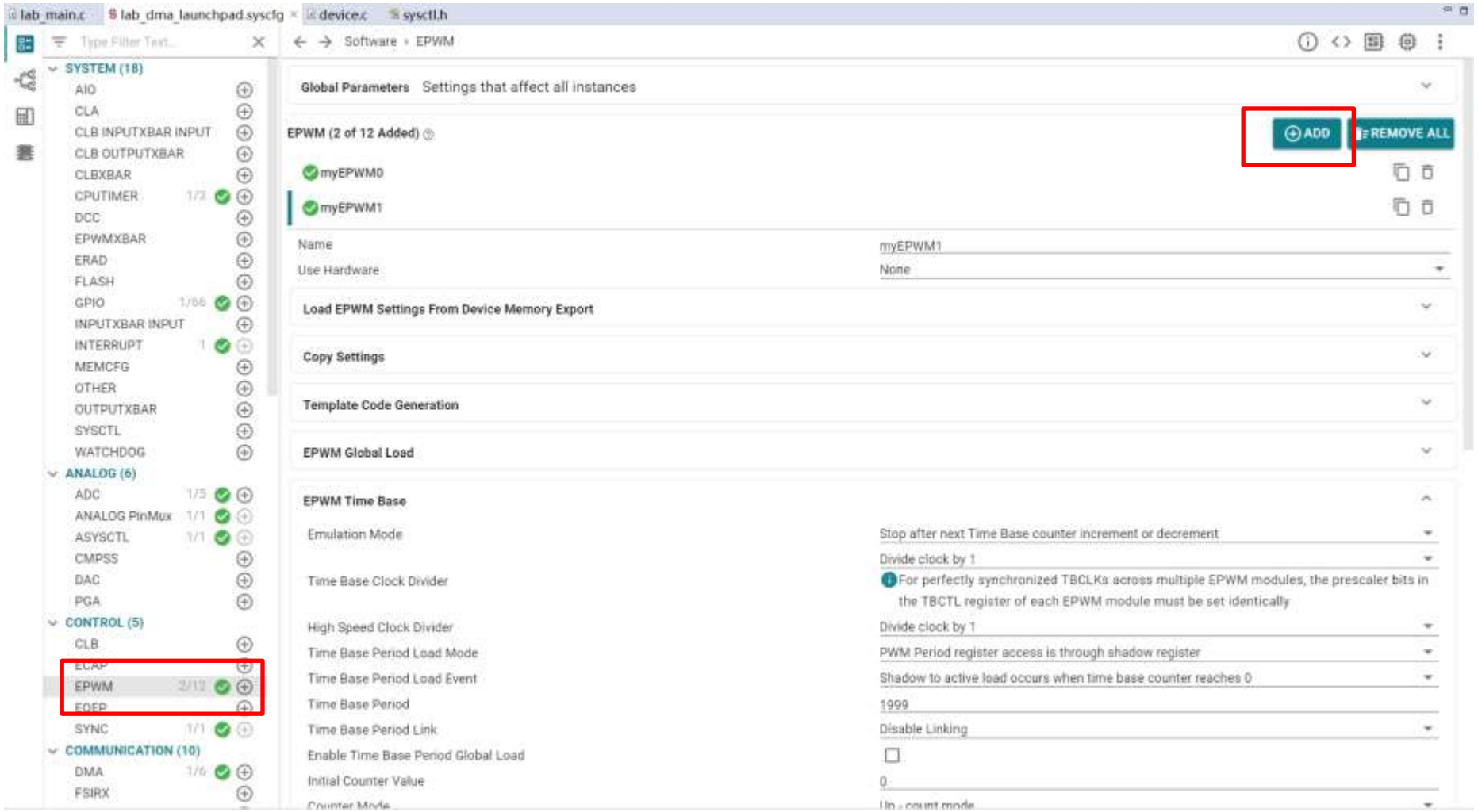
配置EPWM2



DMA

配置EPWM2

EPWM Time Base

Emulation Mode	Stop after next Time Base counter increment or decrement
Time Base Clock Divider	Divide clock by 1 For perfectly synchronized TBCLKs across multiple EPWM modules, the prescaler bits in the TBCTL register of each EPWM module must be set identically
High Speed Clock Divider	Divide clock by 1
Time Base Period Load Mode	PWM Period register access is through shadow register
Time Base Period Load Event	Shadow to active load occurs when time base counter reaches 0
Time Base Period	1999
Time Base Period Link	Disable Linking
Enable Time Base Period Global Load	☐
Initial Counter Value	0
Counter Mode	Up - count mode
Enable Phase Shift Load	☐
Force a Sync Pulse	☐
Sync In Pulse Source	Sync-in source is EPWM1 sync-out signal
Sync Out Pulse	None
One-Shot Sync Out Trigger	Trigger is OSHT sync
EPWMxSYNCPER Source Select	Counter equals Period

$$\text{Time Base Period} = \frac{f_{tbclk}}{2f_{pwm}} = \frac{100*10^6}{2*25000} = 2000.$$

DMA

配置EPWM2

EPWM Event-Trigger

Enable EPWM Interrupt: ☐

ADC SOC Trigger

SOCA Trigger Enable	☑
SOCA Trigger Source	Time-base counter equal to zero or period
SOCA Trigger Event Count	1 Event Generates Interrupt
SOCA Trigger Event Count Initial Value Load Enable	☐
SOCB Trigger Enable	☐

HRPWM

PinMux Use Case: ALL

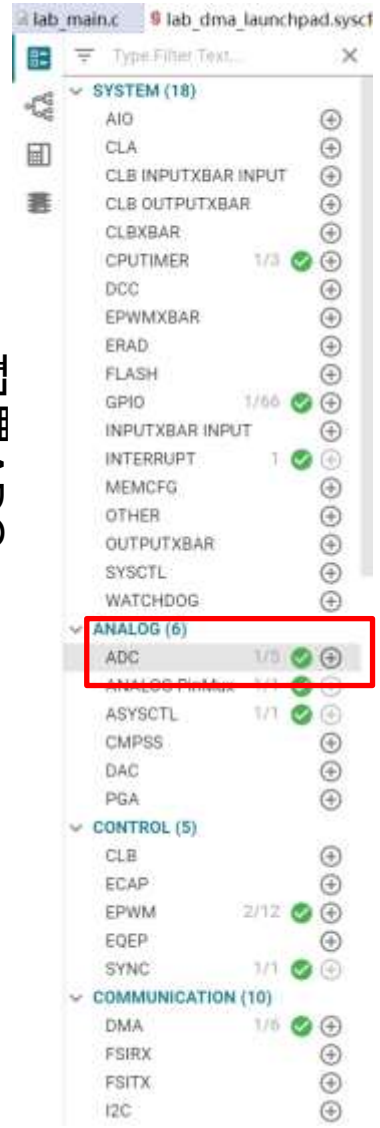
PinMux Qualification

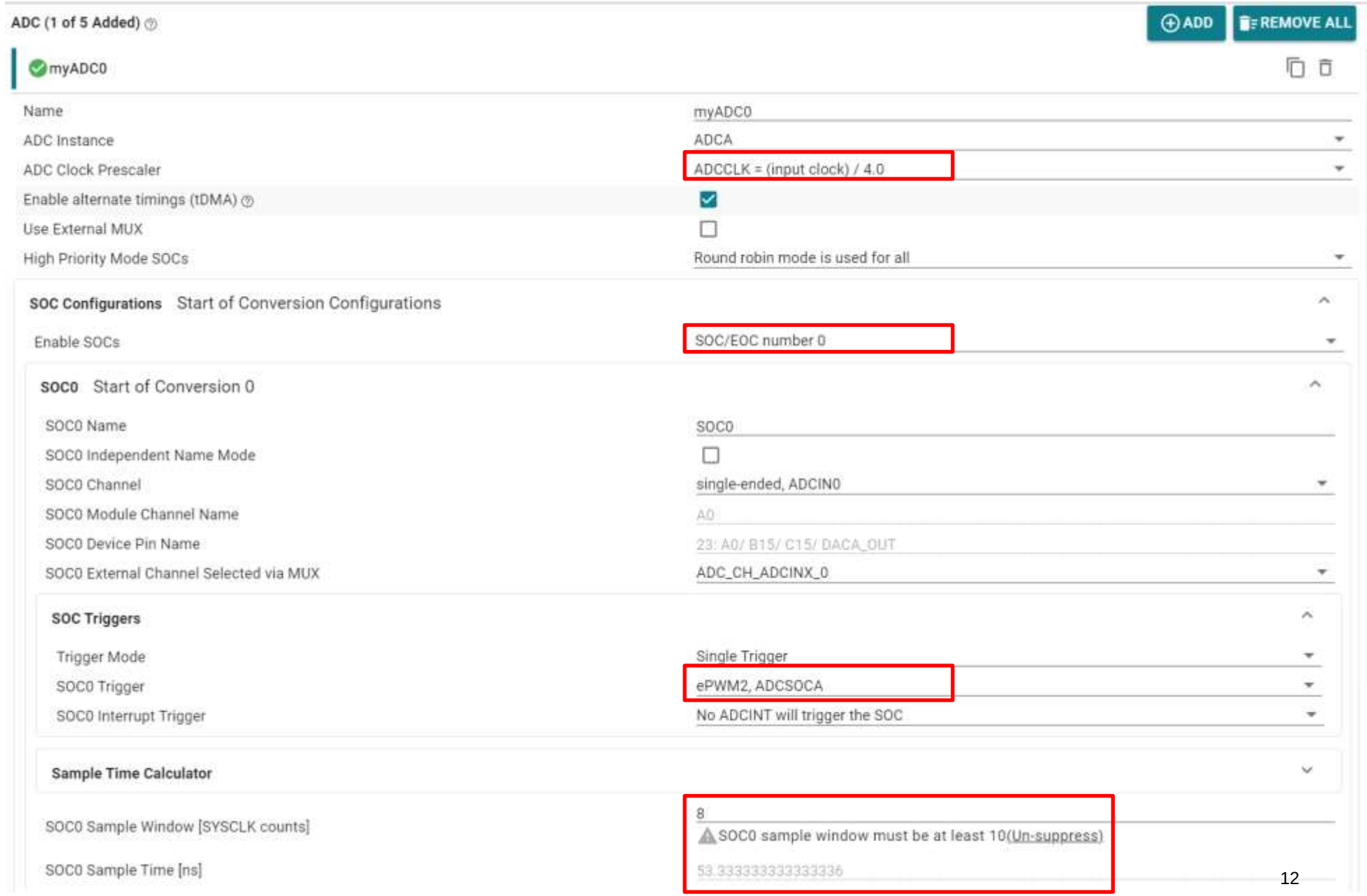
PinMux Peripheral and Pin Configuration

EPWM Peripheral	EPWM2
EPWM_A	GPIO2/77 (EPWM2 BP) ⚠ Connected to hardware(Un-suppress)
EPWM_B	GPIO3/76 (EPWM2 BP) ⚠ Connected to hardware(Un-suppress)

DMA

配置ADC





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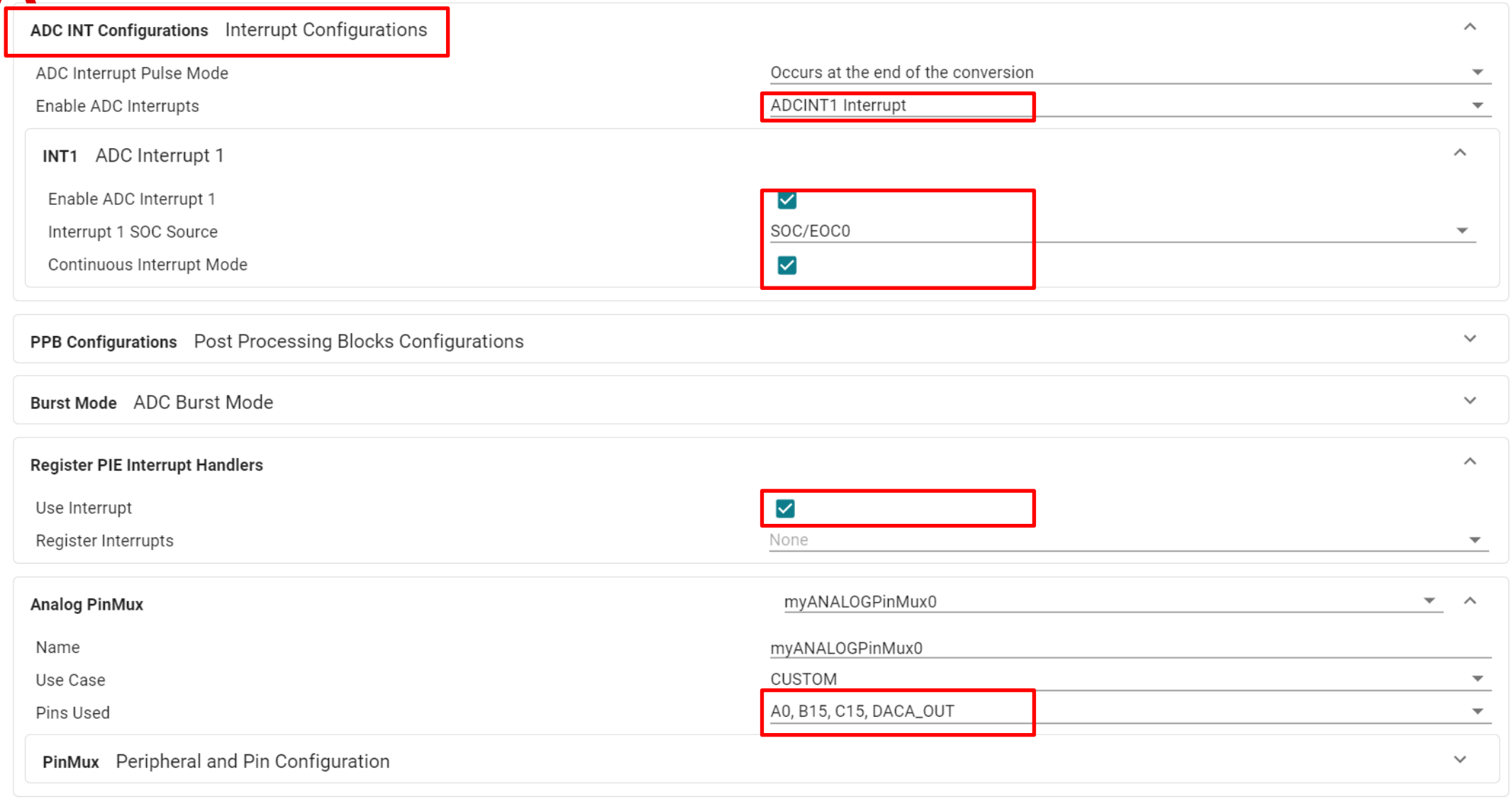
配置ADC



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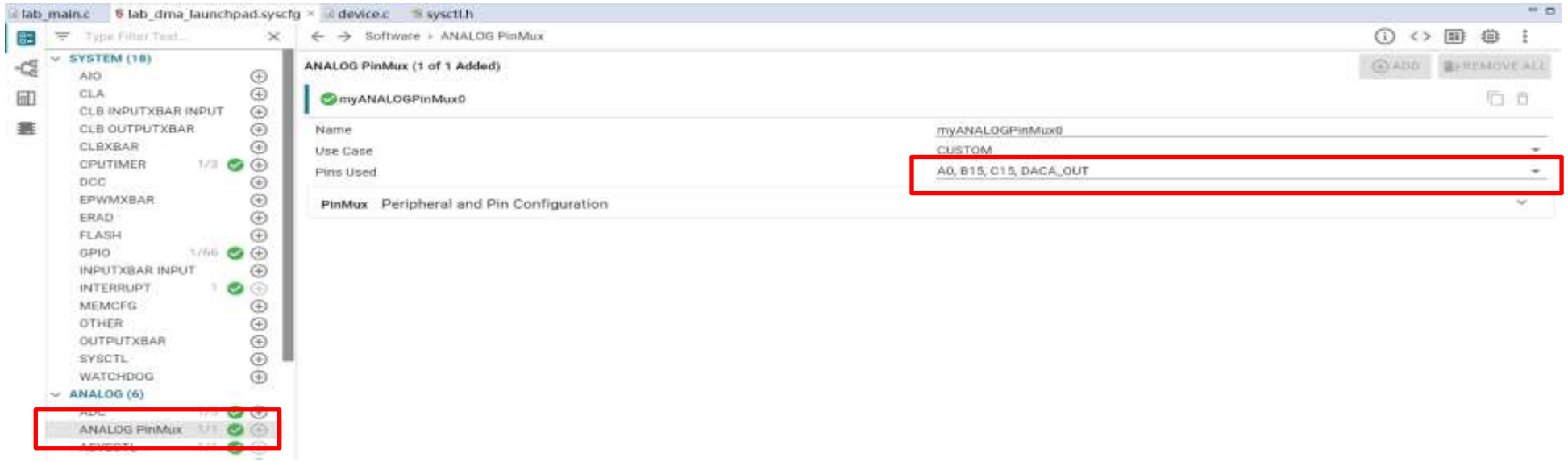
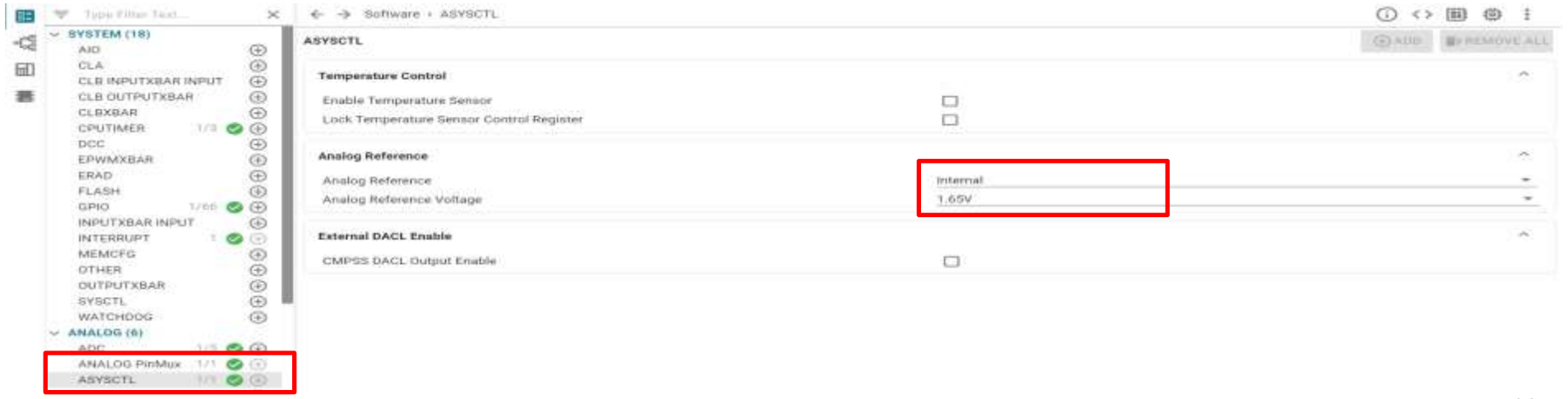
配置ADC





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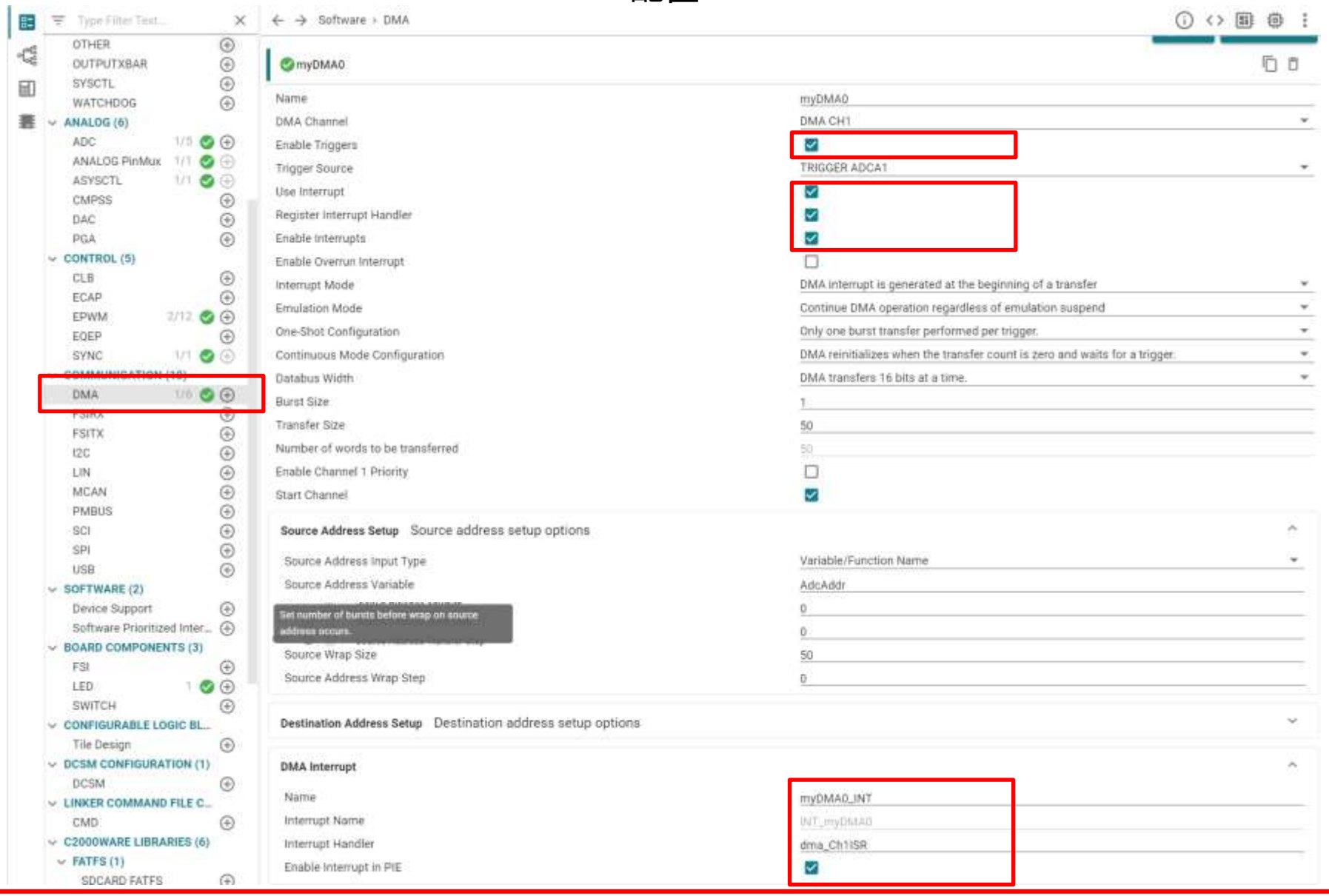
配置DMA



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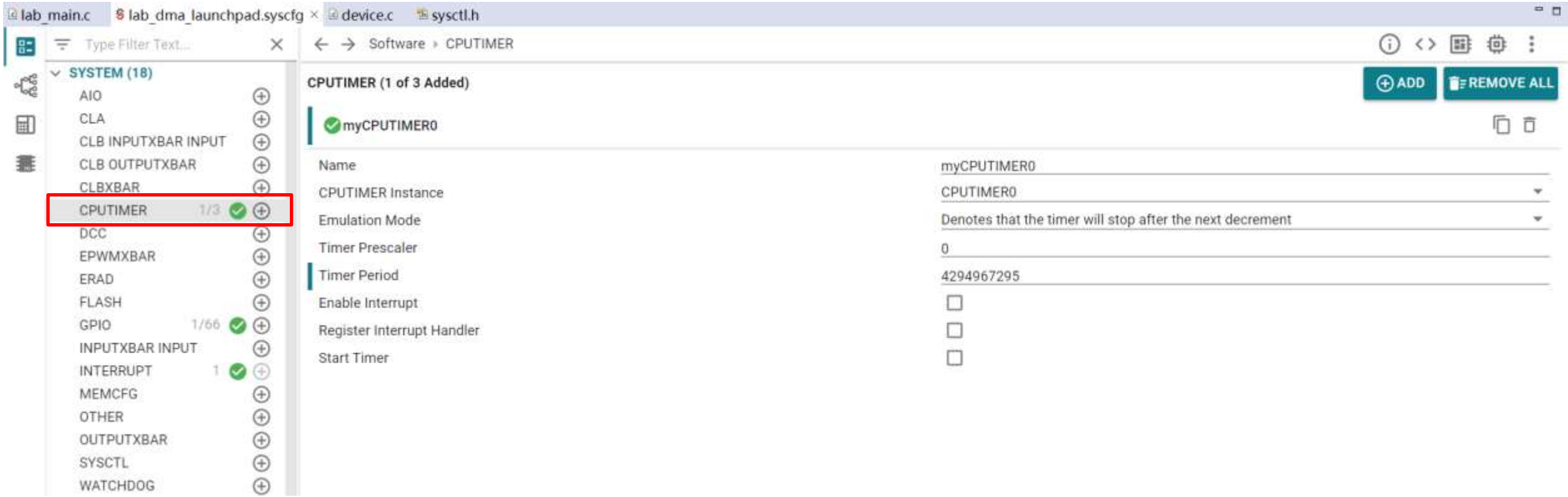
配置Timer



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