

MSPM0 Low-power mode introduction

— MSPM0 peripheral training series

Presented by Eason Zhou

MCU level overview

—MSPM0Gxx series

| MSPM0G350x/310x/150x/110x | | |
|---|-----------------------------|----------------------------------|
| 1.62 - 3.6V -40 to 125 C | | |
| CPU Arm Cortex-M0+ 80 MHz NVIC / MPU / 7-ch DMA | Power & Clocking | Precision Analog |
| | POR / BOR / SVS | 12-bit ADC 4Msps (9-ch) |
| | External LF 32kHz XTAL | 12-bit ADC 4Msps (8-ch) |
| | External HF 4-48MHz XTAL | Comparators w/ 8-bit DACs (3) |
| | Internal LF 32kHz (3%) | 12-bit 1Msps buffered DAC (1) |
| | Internal HF 4-32MHz (1%) | Zero-drift chopper op-amps (2) |
| | PLL (up to 80 MHz) | Internal reference (1.5%) |
| | | General purpose amp (1) |
| | | Temperature sensor |
| Accelerators | Communication | Timers |
| Math (DIV, SQRT, TRIG, MAC) | UART w/ LIN (1) | Advanced control 16-bit 4 CC (1) |
| | UART (3) | Advanced control 16-bit 2 CC (1) |
| On-chip Memory | SPI (2) | General purpose 32-bit 2 CC (1) |
| 32, 64, or 128 kB flash [ECC] | I2C (2) w/ FastMode+ | General purpose 16-bit 2 CC (2) |
| 16 or 32 kB SRAM [ECC] | CAN-FD (1) | Low power 16-bit 2 CC (2) |
| Data Integrity & Security | | Windowed watchdog (2) |
| CRC accelerator (16 and 32 bit) | IO | Real-time clock (1) |
| AES256 accelerator + TRNG | Up to 60 GPIO | |
| Programming & Debug | | |
| ARM SWD interface | | |
| UART & I2C bootloader | | |

Leaded packages: VSSOP-20/28, LQFP-48/64
No-lead packages: VQFN-24/32/48, nFBGA-64, WCSP-28

Power management and clock unit (PMCU)

- System Controller (SYSCTL)
- Power Management (PMU)
- Clock Module (CKM)

80 MHz MCU with up to 128kB flash, 64 pins, advanced analog, AES/TRNG, CAN-FD

MSPM0 PMCU overview

PMCU Introduction

Power management and clock unit (PMCU):

- Provides power, clocking, reset, and system control services for MSPM0
- contains three submodules: SYSCTL, PMU, CKM

System controller (SYSCTL):

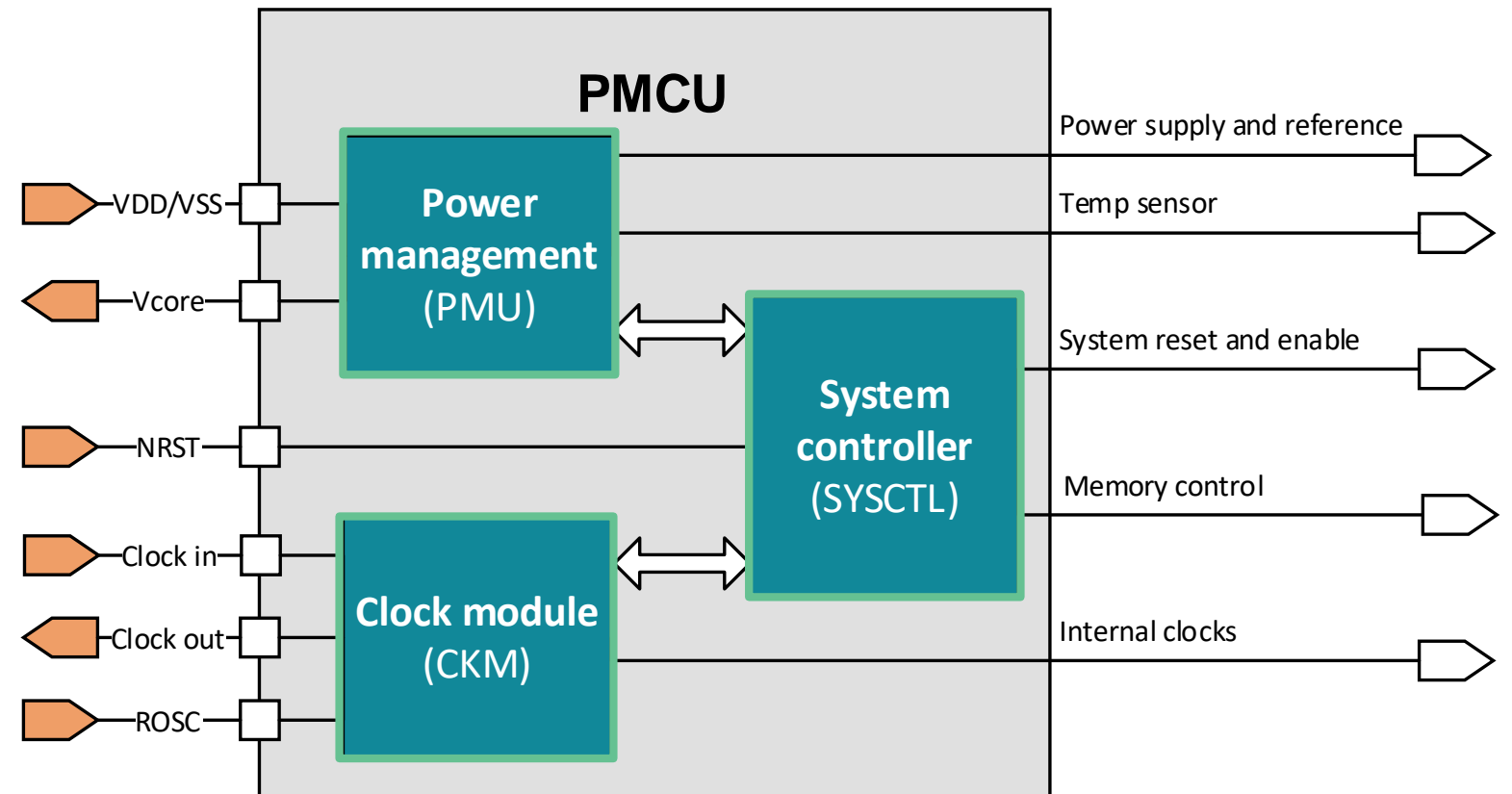
- PMU and CKM configuration
- Peripherals reset and enable
- CPU reset and enable
- Flash and SRAM control

Power management (PMU):

- Power supply to PD0 peripherals and PD1 peripherals
- Power supply to GPIO
- Power supply to analog peripherals
- Voltage reference
- Temperature sensor

Clock module(CKM):

- Clock supply



Low-power mode introduction

PD0 and PD1 Introduction

PD0 domain:

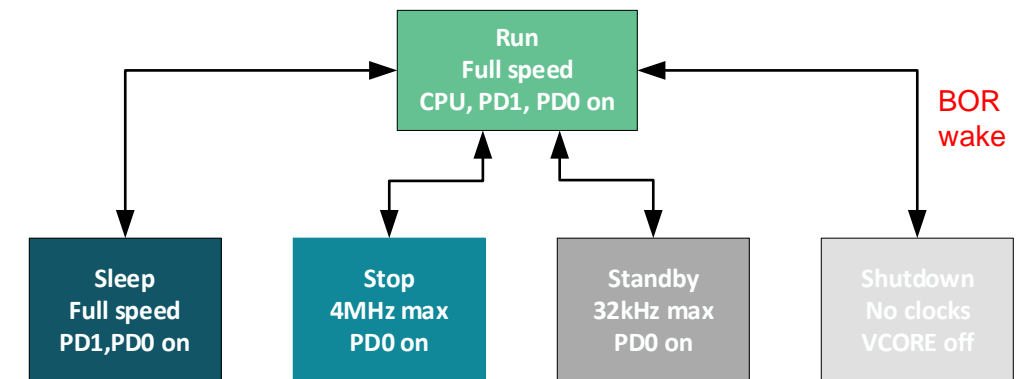
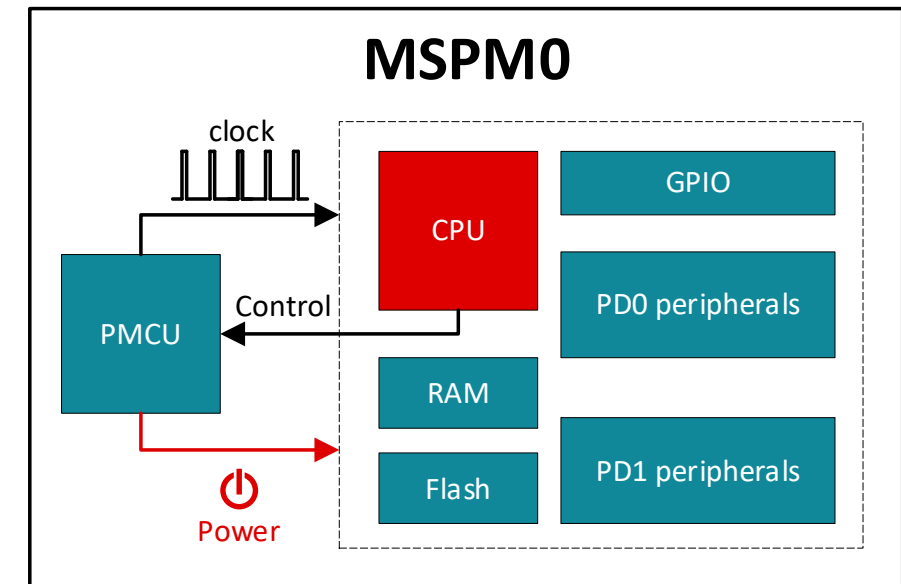
- Includes the PD0 peripherals (I2C / OPA / Timer) and PD0 peripheral bus

PD1 domain:

- Include the CPU sub system, SRAM, Flash, PD1 peripherals (SPI / DMA / ADC / Timer) and the PD1 peripheral bus

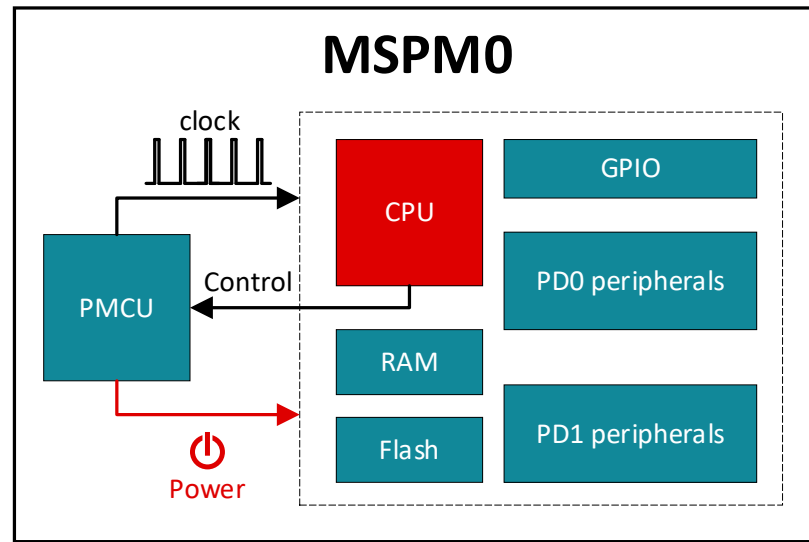
Power Mode Introduction

| Power Mode | Max Frequency | Base Idd | Functionality |
|------------|-----------------|-----------|---|
| RUN | 24 / 32 / 80MHz | ≈85μA/MHz | <ul style="list-style-type: none"> CPU is running All clocks and peripherals are available |
| SLEEP | 24 / 32 / 80MHz | ≈200μA | <ul style="list-style-type: none"> Only CPU is disabled All clocks are available |
| STOP | 4MHz | ≈50μA | <ul style="list-style-type: none"> PD0 peripherals are available PD1 peripherals are disabled with retention Available clocks: MFCLK (4MHz) or LFCLK (32KHz) |
| STANDBY | 32KHz | ≈1μA | <ul style="list-style-type: none"> PD0 peripherals are available PD1 peripherals are disabled with retention Flash and SRAM is disabled with retention Available clock: LFCLK (32KHz) |
| SHUT DOWN | No clocks | ≈50nA | <ul style="list-style-type: none"> All PD0 / PD1 peripherals are off Flash and SRAM are off Only NRST pin and wakeup IOs can wake MSPM0 No available clock |

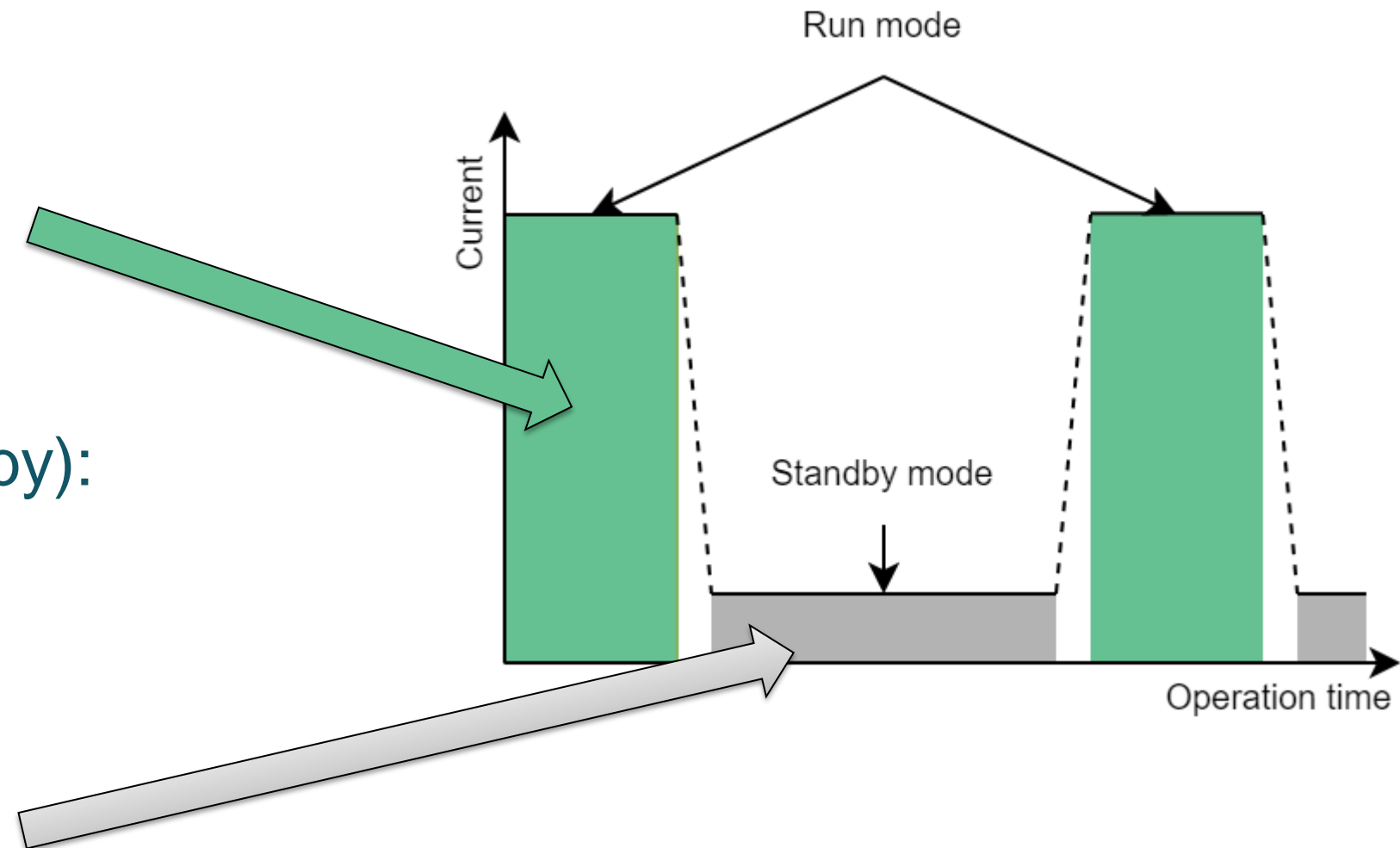
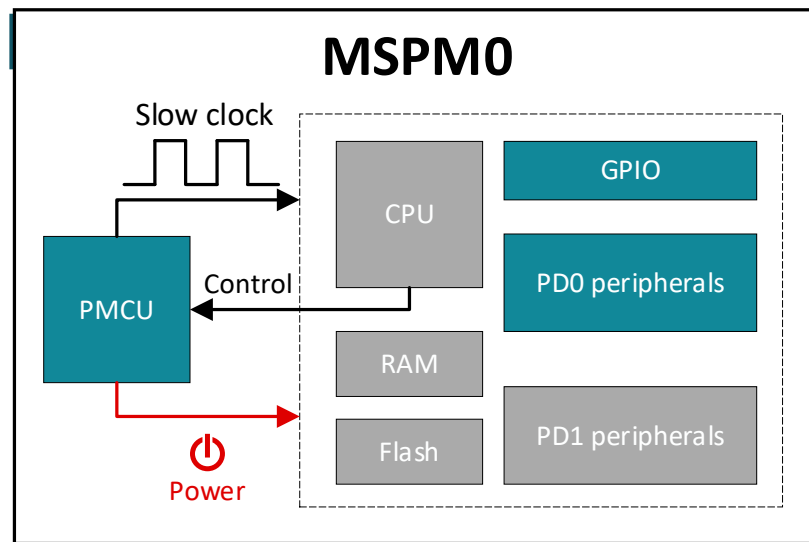


Power mode usage

- Run mode:



- Low-power mode (Standby):



MSPM0 Reset level introduction

POR and BOR Introduction

Power-on reset (POR):

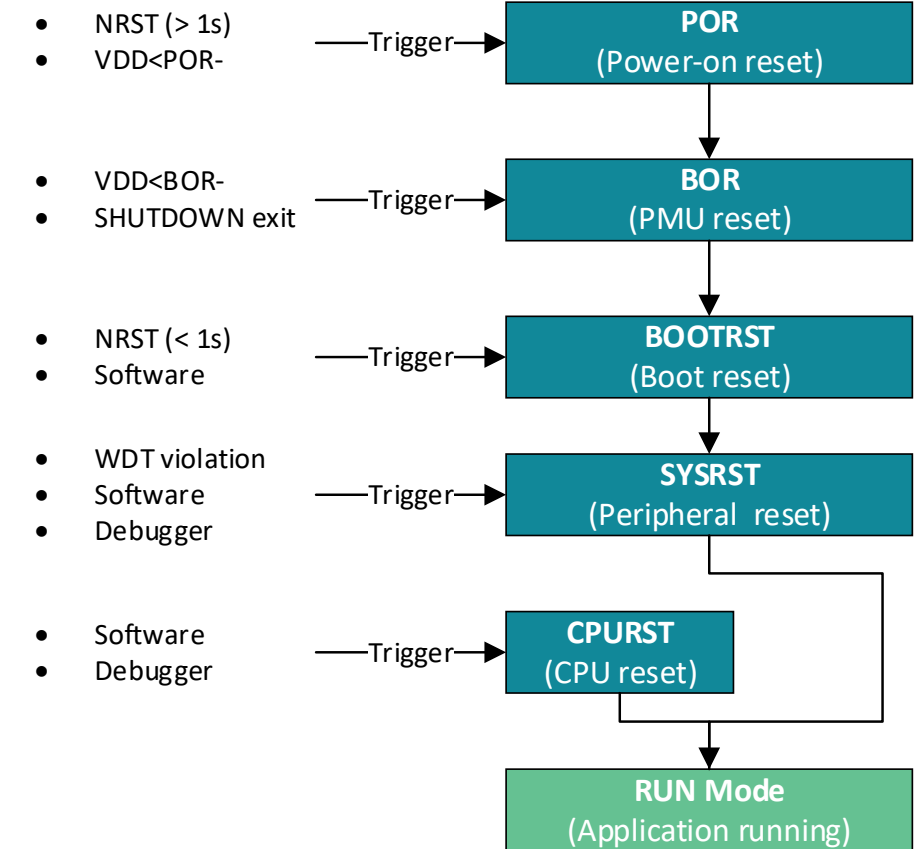
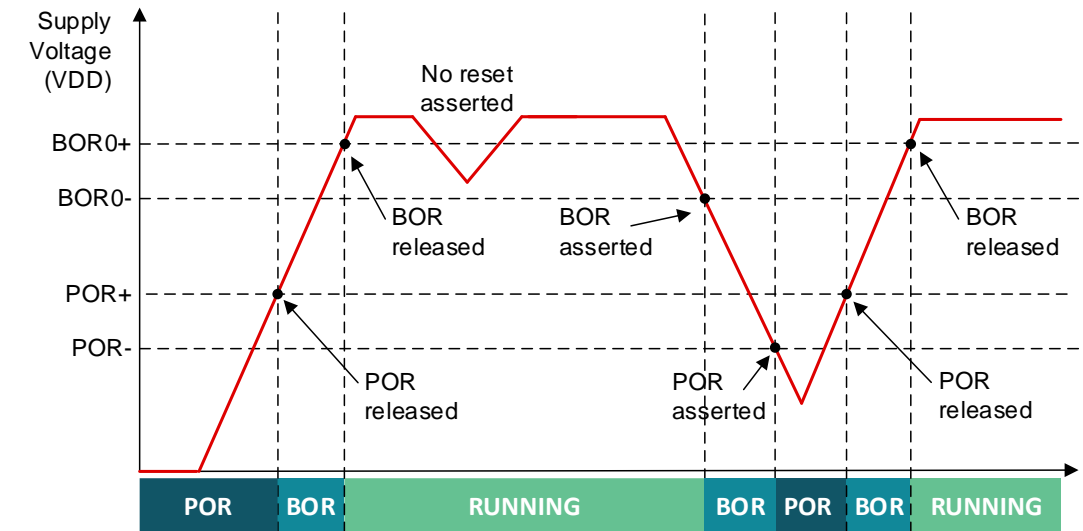
- Indicate VDD has reached sufficient voltage to start BOR circuit

User-programmable brownout reset (BOR):

- Ensures VDD is maintained at a sufficient voltage to support correct operation of the device
- Four selectable BOR threshold levels (BOR0-BOR3)

Reset Level Introduction

| Reset name | Trigger examples | Effect |
|--------------------------|---|---|
| POR (Power-on reset) | <ul style="list-style-type: none"> • NRST (> 1s) • VDD < POR- | <ul style="list-style-type: none"> • Reset shutdown memory • Re-enable NRST/SWD pin function • Trigger BOR |
| BOR (brownout reset) | <ul style="list-style-type: none"> • VDD < BOR- • SHUTDOWN exit | <ul style="list-style-type: none"> • Reset PMU • Reset all of the core logic • Trigger BOOTRST |
| BOOTRST (Boot reset) | <ul style="list-style-type: none"> • NRST (< 1s) • Software | <ul style="list-style-type: none"> • Execute device boot configuration routine • Reset the majority of the core logic • Clear SRAM • Trigger SYSRST |
| SYSRST (System reset) | <ul style="list-style-type: none"> • WDT violation • Software • Debugger | <ul style="list-style-type: none"> • Reset CPU • Reset peripherals |
| CPURST (CPU reset) | <ul style="list-style-type: none"> • Software • Debugger | <ul style="list-style-type: none"> • Reset CPU |



PMCU module quick start

Academy

[Low-power mode introduction lab](#)

[Driverlib](#) Examples

MSPM0G350x:

- sysctl_power_policy_sleep_to_standby
- sysctl_power_policy_sleep_to_stop
- sysctl_shutdown

MSPM0L13xx:

- sysctl_power_policy_sleep_to_standby
- sysctl_power_policy_sleep_to_stop
- sysctl_shutdown

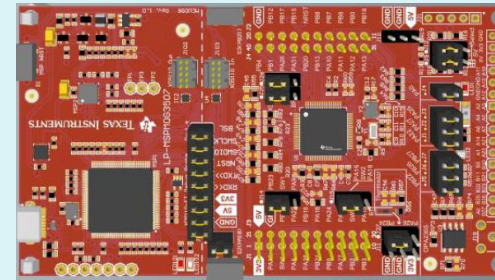
Related Links

- [MSPM0 online resource](#)
- [MSPM0 quick start guide](#)
- [MSPM0 Sysconfig user's guide](#)

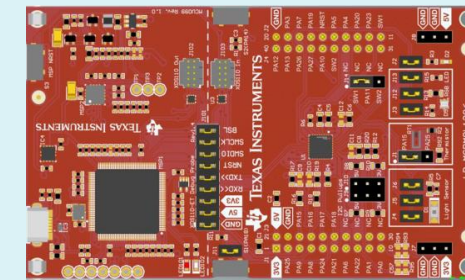
- [MSPM0G350x datasheet](#)
- [MSPM0L13xx datasheet](#)
- [MSPM0Gxx technical reference manual](#)
- [MSPM0Lxx technical reference manual](#)

Launchpad

[LP-MSPM0G3507](#)



[LP-MSPM0L1306](#)



[Sysconfig](#) Entrance for PMCU Setting

The screenshot shows the Sysconfig tool interface. On the left, a tree view under 'MSPM0 DRIVER LIBRARY (7)' shows 'SYSCTL' selected and highlighted with a red box, labeled 'Step 1:'. The main area shows 'SYSCTL' configuration with 'Step 2:' highlighted. The configuration includes 'Power & Systems Configuration' with 'Power Policy' set to 'SLEEPO' and 'BOR Threshold' set to '0'. Other options like 'Enable Write Lock', 'Enable Sleep On Exit', 'Enable Event on Pending', and 'Disable NRST Pin' are shown as unchecked checkboxes. Below this are sections for 'FCC Configuration' and 'Flash Controller (FlashCtl) Configuration'.

To find more MSPM0 training series, please visit:

- [Ti.com.cn](http://ti.com.cn)
- [WeChat \(德州仪器公众号\)](#)
- [Bilibili](#)
- [21IC](#)