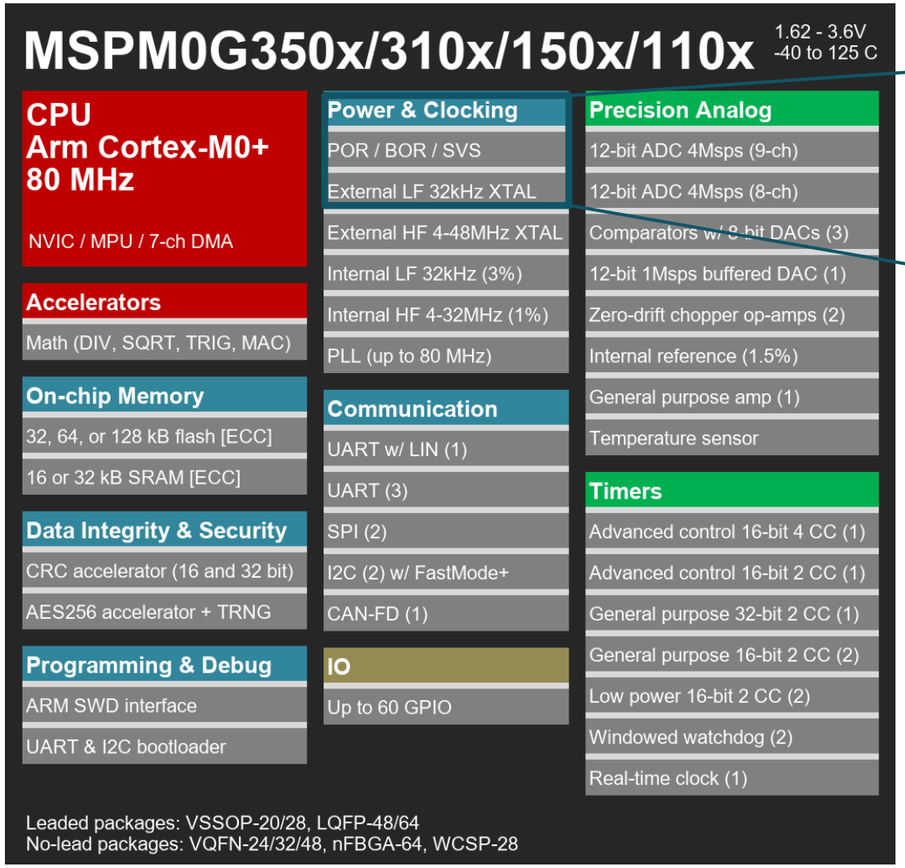
MSPM0 Low-power mode introduction

—— MSPM0 peripheral training series

Presented by Eason Zhou

MCU level overview
——MSPM0Gxx series



Power management and clock unit (PMCU)

- System Controller (SYSCTL)
- Power Management (PMU)
- Clock Module (CKM)

80 MHz MCU with up to 128kB flash, 64 pins, advanced analog, AES/TRNG, CAN-FD

MSPM0 PMCU overview

PMCU Introduction

Power management and clock unit (PMCU):

- Provides power, clocking, reset, and system control services for MPSM0
- contains three submodules: SYSCTL, PMU, CKM

System controller (SYSCTL):

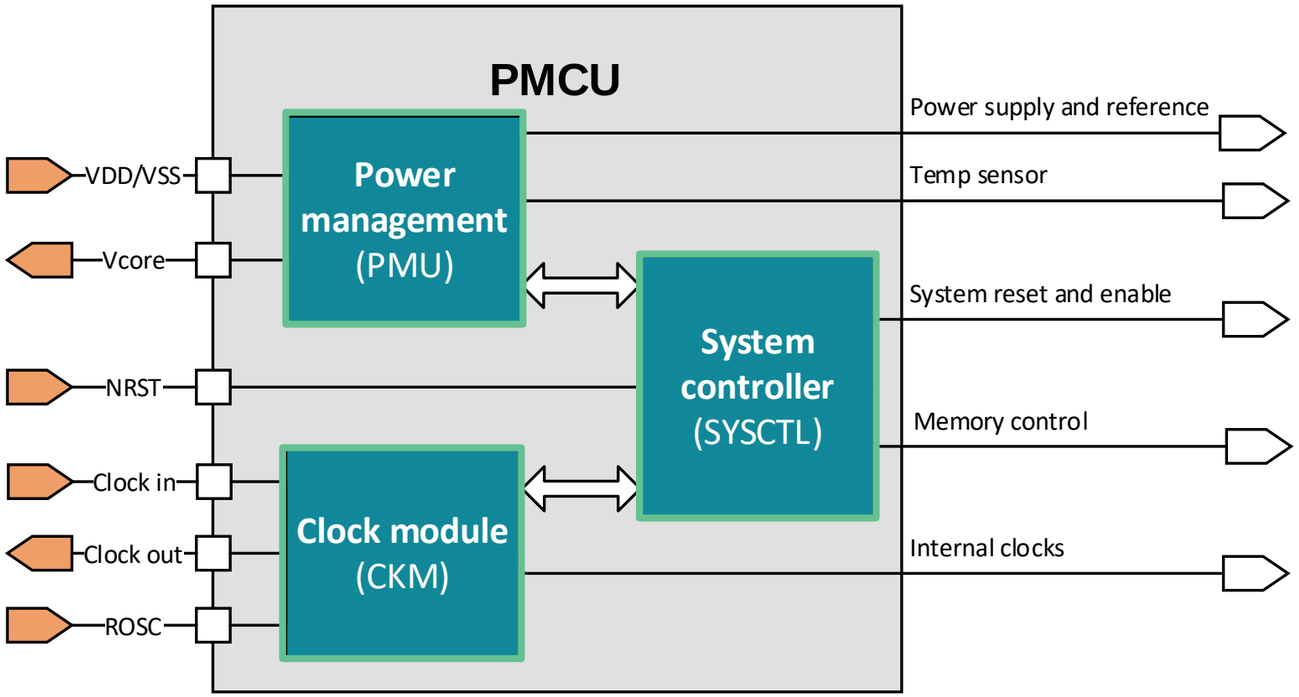
- PMU and CKM configuration
- Peripherals reset and enable
- CPU reset and enable
- Flash and SRAM control

Power management (PMU):

- Power supply to PD0 peripherals and PD1 peripherals
- Power supply to GPIO
- Power supply to analog peripherals
- Voltage reference
- Temperature sensor

Clock module(CKM):

- Clock supply



Low-power mode introduction

PD0 and PD1 Introduction

PD0 domain:

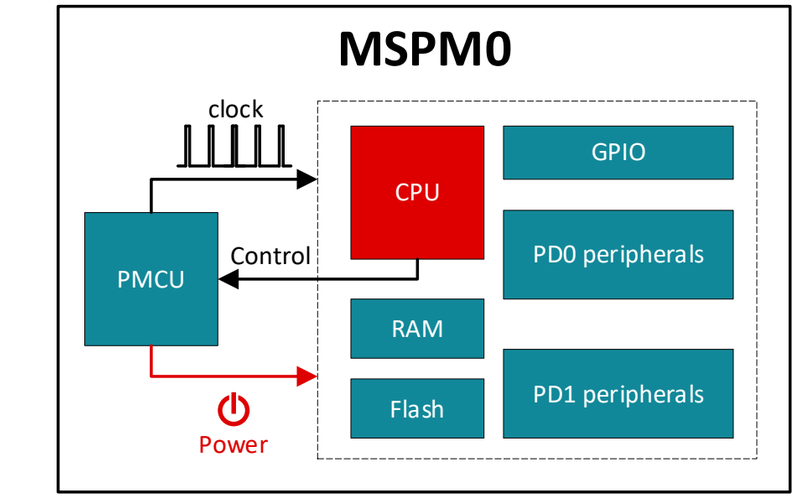
- Includes the PD0 peripherals (I2C / OPA / Timer) and PD0 peripheral bus

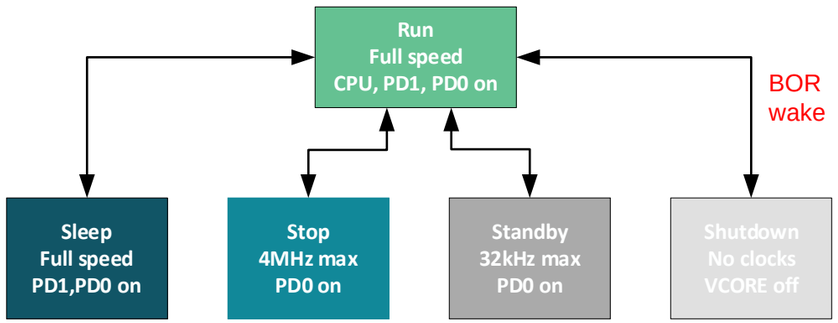
PD1 domain:

- Include the CPU sub system, SRAM, Flash, PD1 peripherals (SPI / DMA / ADC / Timer) and the PD1 peripheral bus

Power Mode Introduction

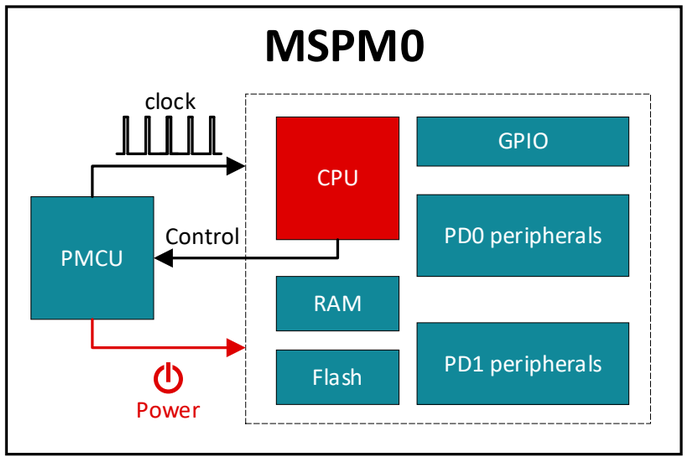
Power Mode	Max Frequency	Base Idd	Functionality
RUN	24 / 32 / 80MHz	≈85µA/MHz	• CPU is running • All clocks and peripherals are available
SLEEP	24 / 32 / 80MHz	≈200µA	• Only CPU is disabled • All clocks are available
STOP	4MHz	≈50µA	• PD0 peripherals are available • PD1 peripherals are disabled with retention • Available clocks: MFCLK (4MHz) or LFCLK (32KHz)
STANDBY	32KHz	≈1µA	• PD0 peripherals are available • PD1 peripherals are disabled with retention • Flash and SRAM is disabled with retention • Available clock: LFCLK (32KHz)
SHUT DOWN	No clocks	≈50nA	• All PD0 / PD1 peripherals are off • Flash and SRAM are off • Only NRST pin and wakeup IOs can wake MSPM0 • No available clock

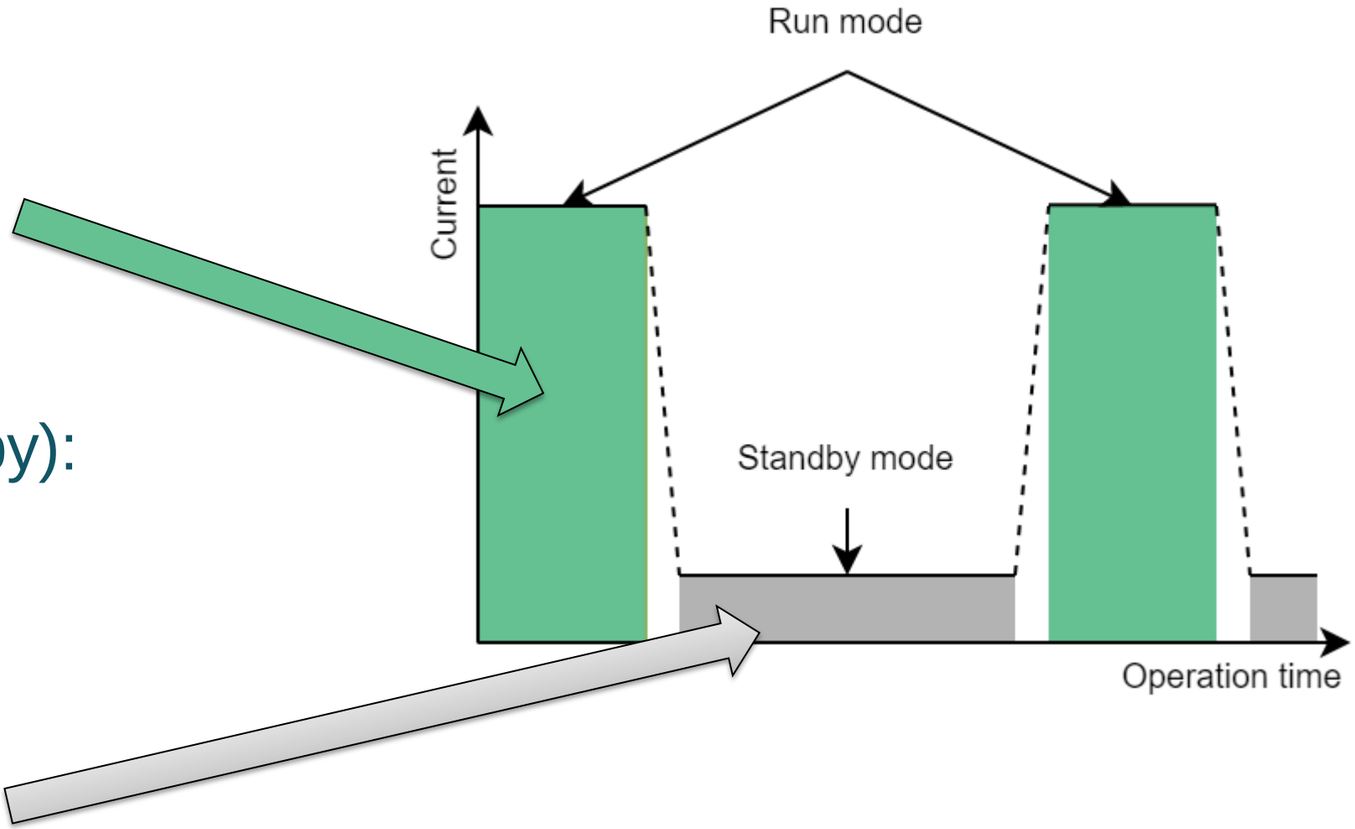




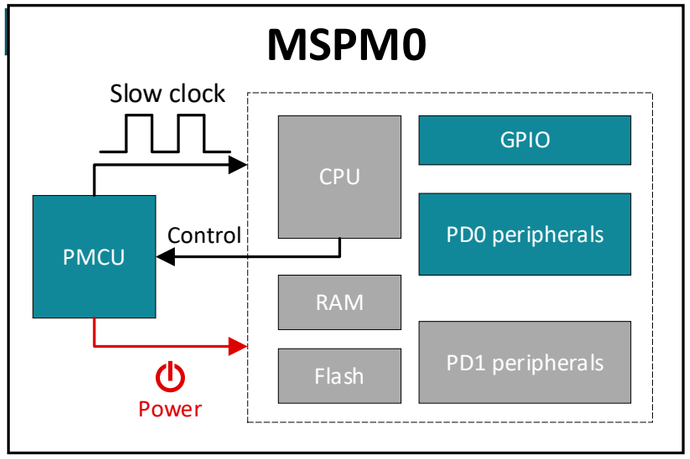
Power mode usage

- Run mode:





- Low-power mode (Standby):



MSPM0 Reset level introduction

POR and BOR Introduction

Power-on reset (POR):

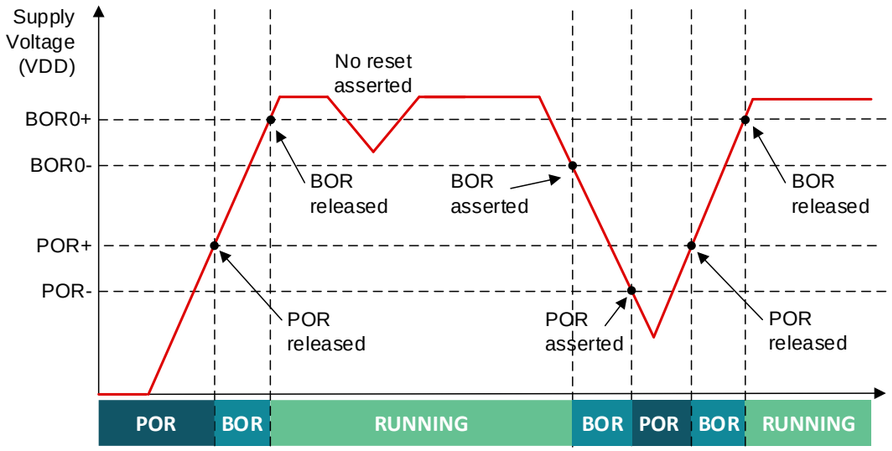
- Indicate VDD has reached sufficient voltage to start BOR circuit

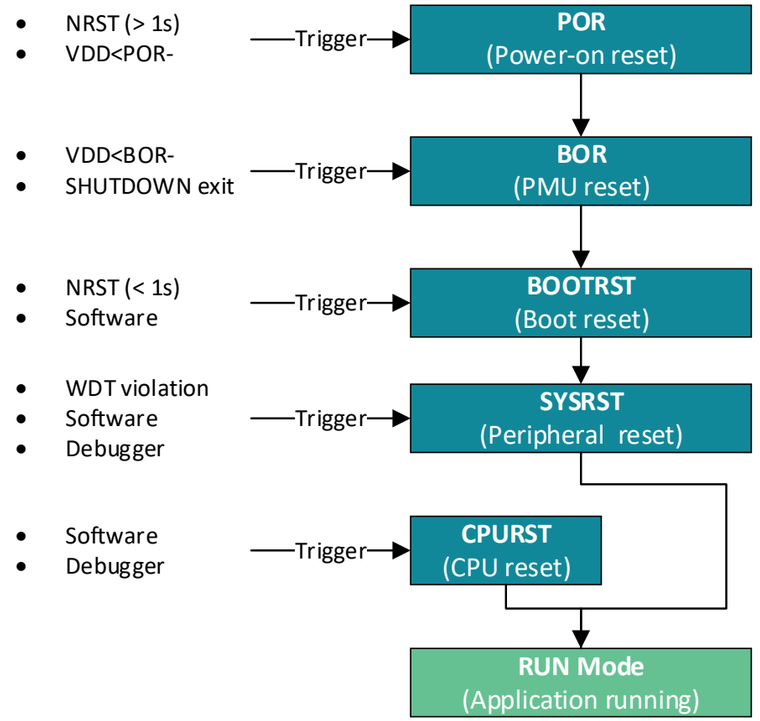
User-programmable brownout reset (BOR):

- Ensures VDD is maintained at a sufficient voltage to support correct operation of the device
- Four selectable BOR threshold levels (BOR0-BOR3)

Reset Level Introduction

Reset name	Trigger examples	Effect
POR (Power-on reset)	• NRST (> 1s) • VDD<POR-	• Reset shutdown memory • Re-enable NRST/SWD pin function • Trigger BOR
BOR (brownout reset)	• VDD<BOR- • SHUTDOWN exit	• Reset PMU • Reset all of the core logic • Trigger BOOTRST
BOOTRST (Boot reset)	• NRST (< 1s) • Software	• Execute device boot configuration routine • Reset the majority of the core logic • Clear SRAM • Trigger SYSRST
SYSRST (System reset)	• WDT violation • Software • Debugger	• Reset CPU • Reset peripherals
CPURST (CPU reset)	• Software • Debugger	• Reset CPU





PMCU module quick start

Academy

Low-power mode introduction lab

Driverlib Examples

MSPM0G350x:

- sysctl_power_policy_sleep_to_standby
- sysctl_power_policy_sleep_to_stop
- sysctl_shutdown

MSPM0L13xx:

- sysctl_power_policy_sleep_to_standby
- sysctl_power_policy_sleep_to_stop
- sysctl_shutdown

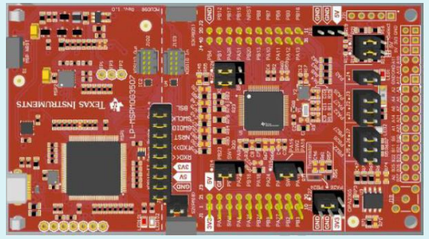
Related Links

MSPM0 online resource
MSPM0 quick start guide
MSPM0 Sysconfig user's guide

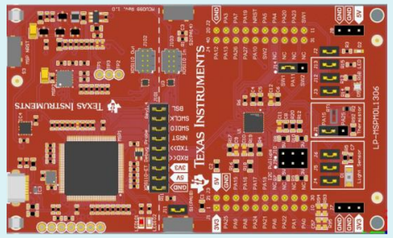
MSPM0G350x datasheet
MSPM0L13xx datasheet
MSPM0Gxx technical reference manual
MSPM0Lxx technical reference manual

Launchpad

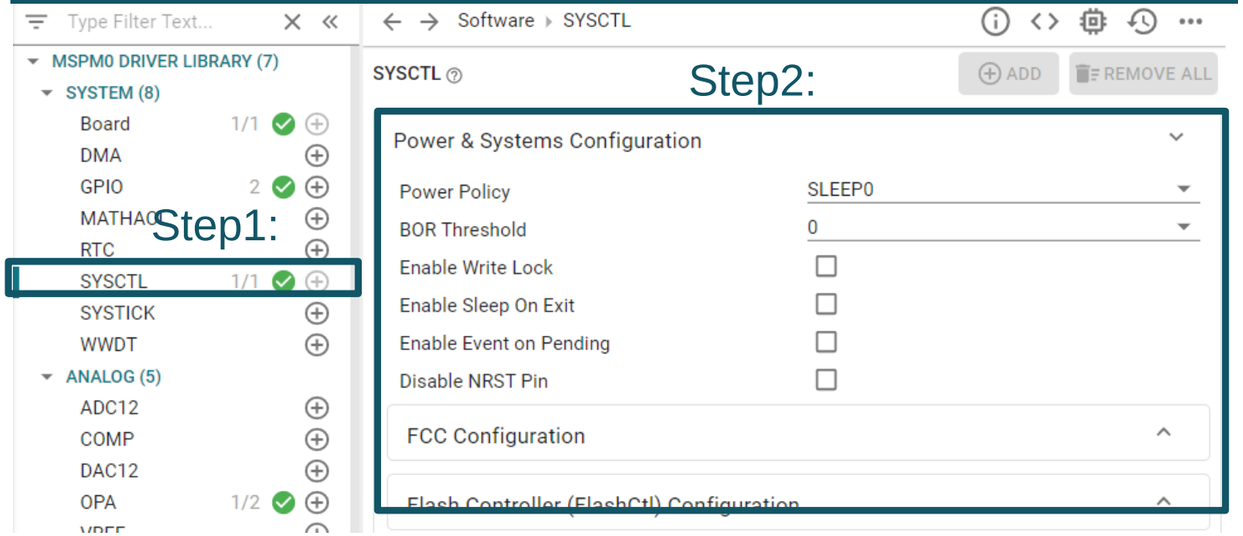
LP-MSPM0G3507



LP-MSPM0L1306



Sysconfig Entrance for PMCU Setting



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- TI.com.cn
- WeChat (德州仪器公众号)
- Bilibili
- 21IC